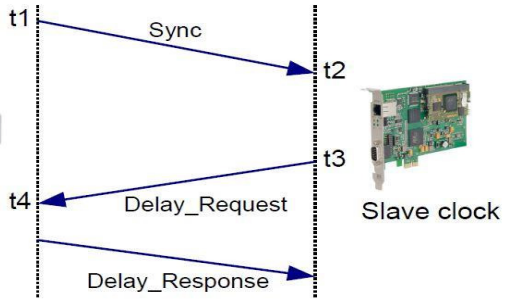
IEEE 1588

- PTP
  - 1588-2002
    - V1
  - 1588-2008
    - V2
  - compatible ?
    - NO, NO, NO!
    - Can co-exist under certain conditions (BC)
    - Careful planning needed
- Purpose
  - To maintain sub ns delay in network
    - Time stamping derived on PHY
      - Independent of CPU load
      - Closest to valid data
    - Caused by:
      - Jitter
      - Cable length
      - Ques in switches
  - Redundancy
  - Use cases
    - Finance and trading
    - Power generation and distribution
    - Industrial automation
    - Telecom
    - Media infrastructure
- Clock types
  - Grand master
    - Selected by BMCA
      - Best Master Clock Algoritm
      - Automatic elevation of master clock
        - Lowest stratum, jitter, etc
    - Usually only one port
  - Ordinary clocks (OC)
    - Master
    - Slave
  - Boundary clocks (BC)
    - Can also be master
    - Measurement point for master
    - Cross network segments
    - Between V1 / V2
      - Seen in DANTE systems
  - Transparent clocks (TC)
    - Not a part of MS, but can be...
      - Behave differently in P2P and E2E
    - Report measured values to each port
- Tech
  - Domains
  - Multicast, but uni possible
  - One/Two step sync
    - Sync
    - Delay_Req
    - Pdelay_Req
    - Pdelay_Resp

Master clock



  - P2P
    - Only use with PTP switches
      - Measured
        - Path delay
        - Resident time
        - Time of flight
        - Both directions, including blocked ports
    - Into
      - http://blog.meinbergglobal.com/2013/09/19/end-end-versus-peer-peer/
  - E2E
    - If even the slightest doubt about switches
      - Calculated on hw level
    - Info
      - http://blog.meinbergglobal.com/2013/09/14/ieee-1588-accurate/