Analog Behavior in Custom IC Variation-Aware Design

(Invited Special Session Paper)

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***Abstract*— This extended abstract describes variation issues in custom integrated circuits (ICs), and how those issues can be addressed via small, specific changes to corner-based design flows. It provides a case study in high-sigma standard cell optimization.**

Keywords—analog circuit; process variation; high-sigma analysis;custom integrated circuit; standard cell; optimization

I. INTRODUCTION

Analysis in the analog domain – continuous values in signals or in time – is necessary not only for classical analog circuits like opamps or bias generators, but also for custom circuits where analog behavior must be considered, including memory cells (bitcells, sense amps) and digital standard cells (NAND gates, flip flops).

Environmental variation (temperature, Vdd, etc.), global process variation, and local process variation (mismatch) have always been around. With each new process node, the effect of variation has multiplied. For example, variance in electrical device performance doubled in one process node step, going from 40nm to 28nm in GF. Figure 1 illustrates. Transistors are getting smaller, but atoms aren't. Gate oxides are only a few atoms thick, so even a few atoms out of place can make a big difference. Atomic variation leads to variation in electrical device performance, which leads to variation in electrical circuit performance at ever-higher levels of hierarchy.

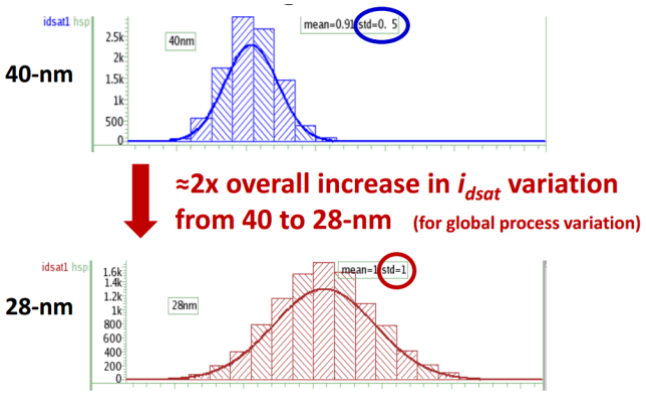

Figure 1: Process Variation: GF 40-nm vs. 28-nm. Increased variation was also observed for mismatch variation, and for global & mismatch combined; for both NMOS and PMOS. From [1].

II. MODERN CORNER-BASED VARIATION-AWARE DESIGN

Variation ultimately hurts yield, or power/performance/area (take your pick – they are flip sides of the same coin). For some circuits, the effect of variation on performance has been long recognized, such as SRAM bitcells or Δ-Σ ADCs. But a simple Monte Carlo (MC) run on virtually any custom circuit will reveal a spread in its outputs, indicating a major effect of process variation on performance.

On modern process nodes from 40 to 28 to 22/20 to 16/14nm, design to handle variation has become essential. There have been many proposals over the years to counter the effects of variation. Revolutionary changes to methodology have been proposed, such as mandating automated sizing or direct MC on response surface models. Fortunately, there's an easier way; no revolution is necessary.

The key is in preserving corner-based design. But now, corners must be better: they must capture the bounds of the circuit performances rather than device performances [2]. Figure 2 illustrates.

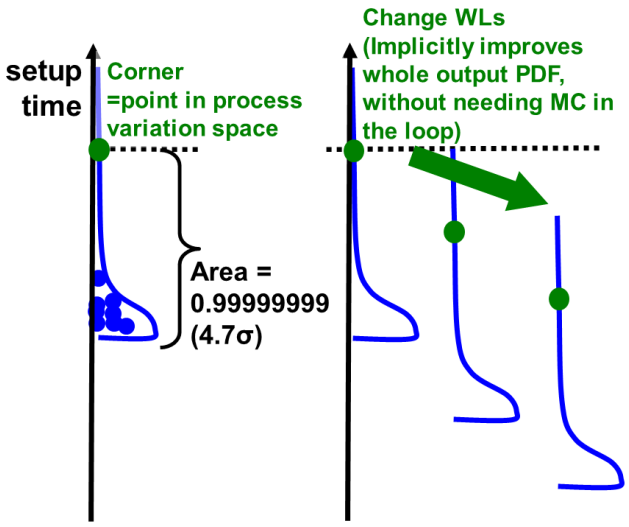

Figure 2: Left: a good statistical corner captures an n-sigma bound of the circuit's performance distribution. Right: improving the design against such a corner implicitly improves the whole distribution.

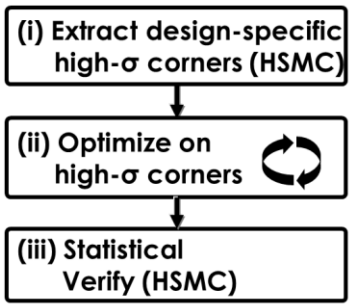

Figure 3: A three-step corner-based variation-aware design flow. One extracts accurate statistical corners, designs on them, and finishes with accurate statistical verification. This variant has high-sigma corners and verification, with automated sizing.

Designing on such "true analog" corners is implicitly "improving performance, subject to 3σ yield" [1,2].

Once the design has been improved against the corners, there must be a more rigorous verification step. For example, one could run Monte Carlo until confident that 3σ yield is met / not met.

Figure 3 illustrates a three-step flow that embodies these aims for high-σ: (i) extract high-σ corners, (ii) design on those corners, and (iii) verify to high-σ. In step (ii), a full statistical analysis is not needed; just corner(s) are simulated. This enables rapid design iterations. Step (iii) is needed in case step (i)'s corners become inaccurate during step (ii) from the interaction between sizing variables and process variables.

Effective variation tools are designed to support each step in the flow well. For each step, variation-aware tools should not only be fast and accurate, they must also be scalable and verifiable. The latter is extremely important: one must be able to trust the tool, and know if the tool has failed. This is akin to SPICE reporting non-convergence in solving for KCL.

Besides the 3σ variation-aware design described above, there is also PVT design, with worst-case performance across PVT corners; and high-σ design for the statistical 4-6 σ level (1/1M to 1/1G failure rates).

III. Case Study: Standard Cell Optimization

For our case study of standard cell optimization, high-σ design is the most appropriate of the possible corner-based variation-aware design flows.

Figure 4 illustrates the three-step approach on the specific case study circuit – minimizing 5σ setup time of a flip flop standard cell. We now elaborate on each step.

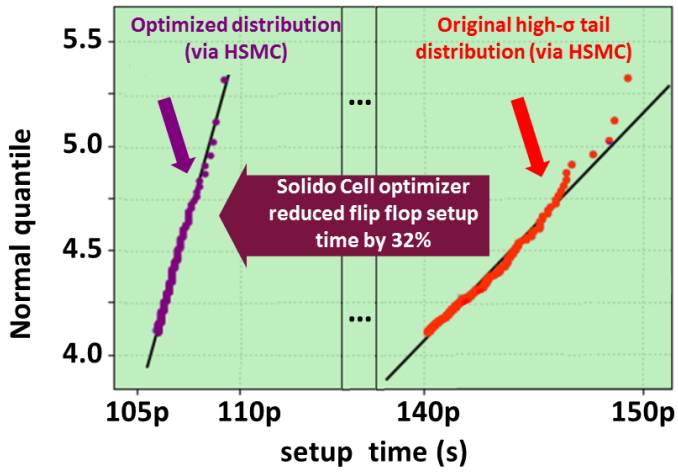

Figure 4: High-σ optimization of a flip flop, via (i) right -- generate original high-σ distribution and extract 5σ corner (ii) middle -- automatically change sizings to minimize setup time at 5σ corner, (iii) left -- run high-σ analysis for final verification. Each step uses SPICE in the loop.

A. *Step (i) – Extract Design-Specific High-σ Corners*

We performed step (i) using Solido High-Sigma Monte Carlo (HSMC) to identify the tail distribution of flip flop setup time.

Figure 5 illustrates the behavior of the HSMC algorithm; [2] provides further detail describing how it is fast, accurate, scalable, and verifiable.

In our case study on the flip flop, HSMC drew 100M MC samples, then used adaptive data mining to identify which tail MC samples to actually simulate. It needed <2000 simulations total.

Figure 4 right illustrates the tail distribution of flip flop setup time, as found by HSMC. Each dot corresponds to an MC sample, a point in process variation space. We retrieved a process point at 5σ (148 ps), to use as a corner.

B. *Step (ii) – Optimize on High-σ Corners*

In the three-step flow, step (ii) can be performed manually or automatically.

Automated sizing is palatable for standard cells because libraries having hundreds of cells may need re-sizing at once, e.g. for porting to a new process or re-optimizing from speed to power; and standard cells have simpler constraints than analog circuits. In our case study, we used Solido Cell Optimizer.

[1] 3σ as in 99.86% overall yield, where "σ" (sigma) is a unit of yield like "probability of failure", not as in 3 standard deviations from mean.
[2] We are not restricted to just 3σ either. It can be 5σ, 6σ, 4.1243σ, or whatever.

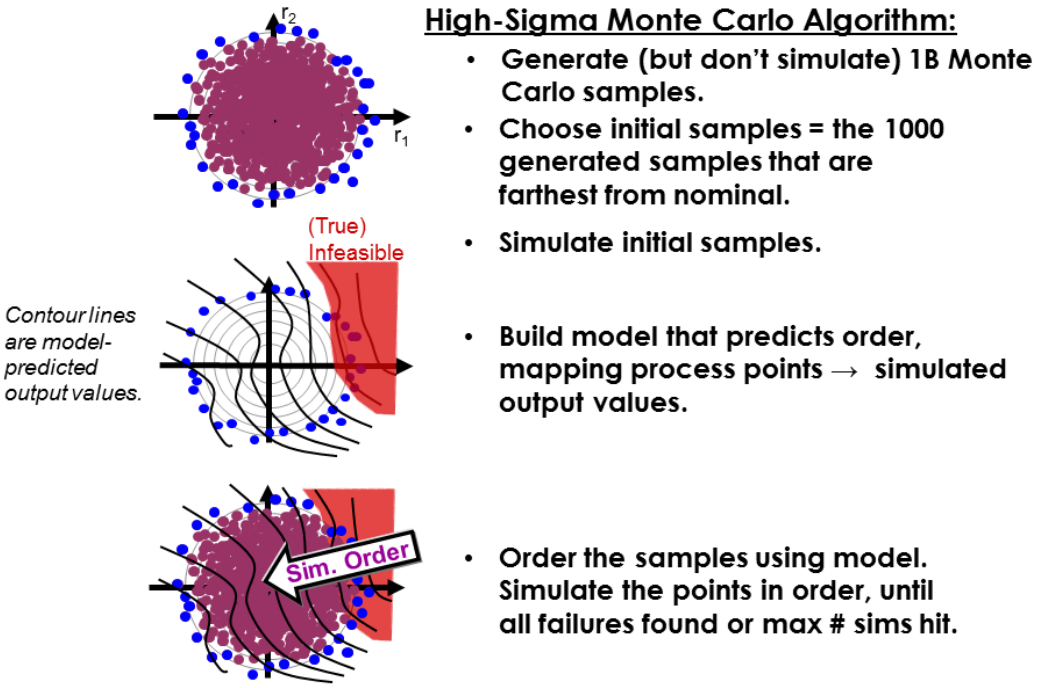

Figure 5: Solido High-Sigma Monte Carlo (HSMC) Algorithm, for verifying circuits and extracting corners at 4-6σ [2].

Figure 6 illustrates the behavior of the Cell Optimizer algorithm [3]. It uses nonlinear regression models [4] to efficiently choose new simulations. To avoid model "blind spots" which could lead to local optima, new simulations are partly chosen based on model uncertainty.

In our flip flop case study, the Cell Optimizer minimized setup time on the 5σ corner from step (i). It took <500 simulations.

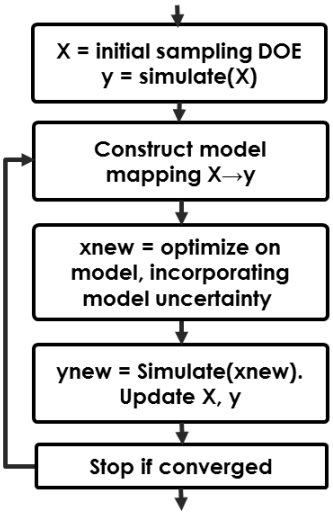

Figure 6: Cell optimizer algorithm

C. *Step (iii) – Statistical Verify*

We performed step (iii) by running Solido HSMC to verify the optimized flip flop design to 5σ. The final setup time tail distribution is shown in Figure 3 left. We see that setup time has reduced by 32% (at 5σ).

IV. Extended Abstract Concluding Remarks

To our knowledge, the flow shown is the only approach to SPICE-accurate high-σ standard cell optimization. More generally, this is the high-σ instance of a variation-aware design methodology in Figure 3.

This methodology can also be applied for 3σ style variation and PVT style variation. To apply to 3σ or PVT design, one simply replaces the high-σ tool with a fast 3σ tool or a fast PVT tool respectively (e.g. Solido Fast MC, Fast PVT [3]). For sizing, one can use manual or automated corner-based tools.

References

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