Sizing mixed-mode circuits by multi-objective evolutionary algorithms

I. Guerra-Gómez[a], E. Tlelo-Cuautle[a], Trent McConaghy[b], Luis G. de la Fraga[c], Georges Gielen[d], G. Reyes-Salgado[e], J.M. Muñoz-Pacheco[f]
[a]INAOE, Department of Electronics. México
[b]Solido Design Automation Inc. Canada
[c]CINVESTAV, Computer Science Department. México
[d]Katholieke Univ Leuven, Dept Elektrotech, ESAT MICAS, B-3001 Louvain, Belgium
[e]CENIDET, Computer Science Department. México
[f]UPP, Electronics and Telecommunications Department, Puebla 72640, México

***Abstract*—We show the behavior of the generations of two multi-objective evolutionary algorithms (MOEAs) for the optimal sizing of two mixed-mode circuits. The non-sorting genetic algorithm (NSGA-II), and the MOEA based on decomposition (MOEA/D) are used to size a second generation current conveyor (CCII+) and a current-feedback operational amplifier (CFOA). Both MOEAs take into account design constraints, and link HSPICE to evaluate the electrical characteristics of the CCII+ and CFOA. Differential evolution is used as genetic operator to show the behavior of the generations of the two MOEAs.**

I. Introduction

Analog signal processing applications require the use of different kinds of active devices. Besides, the majority of the active devices, already known or new ones, can be designed by using four unity-gain cells (UGCs), namely: voltage follower, voltage mirror, current follower, and current mirror [1], [2]. Furthermore, the combination or superimposing of UGCs leads to the generation of mixed-mode circuits such as current conveyors (CCs) [3], and current-feedback operational amplifiers (CFOAs) [2]. Some applications of CCs and CFOAs include sinusoidal and chaotic oscillators [4], [5]. However, to improve the performances of these applications, it is very much needed to optimize the behavior of the mixed-mode circuits.

Although some optimization approaches have been already presented for analog circuits [6]–[8], the sizing-optimization-problem is an unsolved one yet. Besides, the actual tendency is to apply evolutionary algorithms (EAs) [9]–[13], combined with intelligent techniques [6]–[8]. However, there is not information on the behavior of the generations during the sizing process. That information can help an analog integrated circuit designer to select the appropriate tool for the sizing process. In this manner, we show the behavior of the generations by applying the nonsorting genetic algorithm (NSGA-II) [11], and the multi-objective EA based on decomposition (MOEA/D) [9], to size mixed-mode analog circuits such as CCs and CFOAs. The algorithms include differential evolution (DE) as the genetic operator and take into account design constraints, while linking HSPICE to evaluate electrical characteristics.

II. Analog circuit sizing

Analog integrated circuit design is a hard and tedious work due to the large number of parameters, constraints and performances that the designer has to handle [6]–[8], [10]–[13]. As highlighted in [6]–[8], since analog designs are becoming more and more complex, there is a pressing need for analog circuit design automation (ADA), to meet the time to market constraints. In this manner, this work shows the behavior of the generations of NSGA-II and MOEA/D to contribute to solve the sizing problem of mixed-mode circuits. Basically, both EAs search for the optimal width (W) and length (L) of the MOSFETs to accomplish target specifications of a positive-type second generation CC (CCII$^+$), shown in Fig. 1, and a CFOA, shown in Fig. 2. Both algorithms work on a MATLAB code, they include differential evolution (DE) as genetic operator, and the simulations are made with HSPICE. The main goal is to show the behavior of the generations during the sizing process.

The circuit optimization problem is established as follows:

$$\begin{aligned} &\text{minimize f}: \quad \mathbb{R}^n \rightarrow \mathbb{R}^m \\ &\qquad \text{f}(\mathbf{x}) = [f_1(\mathbf{x}), f_2(\mathbf{x}), \ldots, f_m(\mathbf{x})]^{\mathrm{T}} \\ &\text{subject to } h_k(\mathbf{x}) \geq 0, \quad k = 1, \ldots, p, \end{aligned} \tag{1}$$

where n is the size (or number of variables) of the input vector, m is the number of objective functions, $\mathbf{x} = [x_1, x_2, \ldots, x_n]^{\mathrm{T}}$ is the input vector, f is the vector of the objective functions values, and $h_k(\mathbf{x})$, $k = 1, \ldots, p$ are constraints. The simulations are performed by HSPICE LEVEL 49 for standard CMOS technology of 0.18 μm. For the measurements there is a load capacitor of 1 pF.

III. Multi-objective evolutionary algorithms

Evolutionary algorithms, even mixed with other artificial intelligence techniques, are used in multiobjective optimization tools for analog integrated circuits because it makes easy to change the number of objectives or variables and with different magnitudes [8], [12]–[14]. Additionally, they can take into

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account constraints under user defined limits between design parameters and electrical characteristics [15].

The NSGA-II EA [11], is based on Pareto ranking. Fist, it is necessary to built two populations, each one of size N (with N individuals). NSGA-II in each generation rebuild the current population from the two initial populations. After the initialization, the next step is a nondominating sorting process of all solutions in the rebuilt population, which is ranked and classified, acoording to Pareto's dominance, in a family of sub-fronts. Next, it is necessary to choose from the sub-fronts a new offspring of N individuals, in a form that such individuals belong to the first sub-fronts and a distance measure is used to preserve the diversity of the created offspring, by selecting solutions that are far from the rest [11].

The basic idea of MOEA/D [12], is the decomposition of a multiobjective problem in scalar optimization subproblems by a *weights vector* [9]. This vector associates a weight (λ) for each subproblem that is considered as a single solution in the population and is going to try to improve by itself and to its nearby (*neighborhoods*). In each generation there is a population of N solutions $\mathbf{x}^1, \mathbf{x}^2, \ldots, \mathbf{x}^N \in X$ where $\mathbf{x}^i = (x_1^i, \ldots, x_n^i)$ is the current solution to the i_{th} subproblem. After the initialization of the parameters the first step in MOEA/D is related to define the N spread weights vector (to each solution corresponds one λ_i). Therefore, it is possible to define a number (T) of neighborhoods for each λ_i.

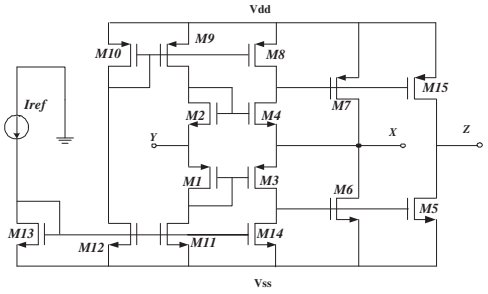

Fig. 1. Current Conveyor (CCII$^+$)

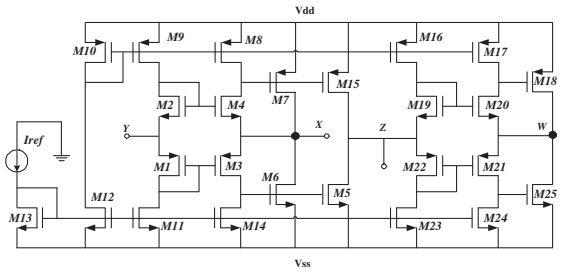

Fig. 2. Current-Feedback Operational Amplifier (CFOA)

In the procedure it is necessary to generate a new solution $\mathbf{y}$ which will be compared with all its neighborhood by applying a decomposition approach and each neighbor worse than this new solution will be replaced by it in an external population (EP) which is used to store non-dominated solutions [12].

IV. Sizing optimization by NSGA-II and MOEA/D

In this section are shown the optimization results for the mixed-mode circuits depicted in Figs 1 and 2. Each one was optimized with different number of variables, objectives, population size and number of generations. Each EA includes DE as the genetic operator.

A. Positive Second Generation Current Conveyor (CCII$^+$)

The CCII$^+$ depicted in Fig. 1 is encoded with nine design variables: transistors lengths (L) and widths (W_i), where i represents a specific transistor (or transistors which share the same width) of the circuit, as shown in Table I.

TABLE I
CCII$^+$ ENCODING

gene	Design Variable	Encoding Transistors
x_1	L	$M_1, \ldots M_{15}$
x_2	W_1	$M_{11}, M_{12}, M_{13}, M_{14}$
x_3	W_2	M_8, M_9, M_{10}
x_4	W_3	M_6
x_5	W_4	M_7
x_6	W_5	M_1, M_3
x_7	W_6	M_2, M_4
x_8	W_7	M_{15}
x_9	W_8	M_5

For this optimization problem, we have 9 variables and 10 objective functions. The domain for the input variables is $x_1 \in \{0.36\ \mu m, 0.54\ \mu m, 0.72\ \mu m\}$, $x_i \in [0.36\ \mu m, 80\ \mu m]$, for $i \in [2, \ldots, 9]$ and the ten objectives are:

- $f_1(\mathbf{x}) = 1 -$ (voltage gain); from port Y to port X.
- $f_2(\mathbf{x}) =$ (voltage offset); between port Y and port X.
- $f_3(\mathbf{x}) = 1/$(voltage band width); from port Y to port X.
- $f_4(\mathbf{x}) = 1/$(input resistance); in port Y.
- $f_5(\mathbf{x}) =$ (output resistance); in port X.
- $f_6(\mathbf{x}) = 1 -$ (current gain); from port X to port Z.
- $f_7(\mathbf{x}) =$ (current offset); between port X and port Z.
- $f_8(\mathbf{x}) = 1/$(current band width); from port X to port Z.
- $f_9(\mathbf{x}) =$ (input resistance); in port X.
- $f_{10}(\mathbf{x}) =$ (output resistance); in port Z.

In our experiments we include the saturation condition in all transistors as constraints. Then this circuit was optimized along 111 generations over 10 runs, with a population size for 111 by using DE [12].

TABLE II
NSGA-II OPTIMIZATION RESULTS FOR THE CCII$^+$

	GainV ($\frac{V}{V}$)	OffsetV (V)	BWV (Hz)	RoutV (Ω)	RinV (Ω)
MAX	0.9885	4.836e-003	9.733e+008	3.1576	8.115e+004
MIN	0.9758	1.105e-004	5.268e+008	0.6239	7.393e+003
AVG	0.9858	2.159e-003	7.913e+008	1.1510	2.783e+004
STD	1.947e-003	7.562e-004	1.308e+008	0.4134	1.788e+004
	GainI ($\frac{I}{I}$)	OffsetI (A)	BWI (Hz)	RoutI (Ω)	RinI (Ω)
MAX	0.9999	4.988e-005	9.425e+008	1.456e+005	13.8628
MIN	0.8513	1.972e-008	2.218e+008	7.758e+003	0.8994
AVG	0.9302	1.878e-005	4.917e+008	2.504e+004	2.5182
STD	4.140e-002	1.402e-005	1.130e+008	2.406e+004	2.4096

Figures 3 and 4 depict the behavior of the best values in each generation of the CCII$^+$ optimization for NSGA-II and MOEA/D, respectively. Tables II and III show the maximum, minimum, average and standard deviation values for NSGA-II and MOEA/D in the optimal sizing of the CCII$^+$.

B. Current Feedback Operational Amplifier (CFOA)

The CFOA depicted in Fig. 2 is encoded with fifteen design variables: transistors lengths (L) and widths (W_i), where i represents a specific transistor (or transistors which

TABLE III
MOEA/D OPTIMIZATION RESULTS FOR THE CCII$^+$

	GainV ($\frac{V}{V}$)	OffsetV (V)	BWV (Hz)	RoutV (Ω)	RinV (Ω)
MAX	0.9897	6.129e-003	9.734e+008	20.8758	1.011e+005
MIN	0.9592	7.773e-007	2.650e+008	0.5303	6.552e+003
AVG	0.9856	1.548e-003	7.268e+008	1.7078	5.037e+004
STD	5.076e-003	1.108e-003	1.551e+008	2.1357	2.873e+004
	GainI ($\frac{I}{I}$)	OffsetI (A)	BWI (Hz)	RoutI (Ω)	RinI (Ω)
MAX	1.0000	4.994e-005	9.832e+008	5.142e+005	65.3312
MIN	0.8514	6.135e-010	1.175e+008	6.641e+003	0.6405
AVG	0.9605	1.421e-005	5.175e+008	3.251e+004	4.2372
STD	4.911e-002	1.392e-005	1.680e+008	5.645e+004	8.3924

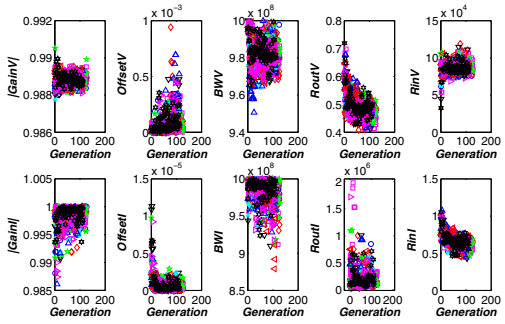

Fig. 3. Generation VS Objectives for NSGA-II for CCII$^+$ Optimization

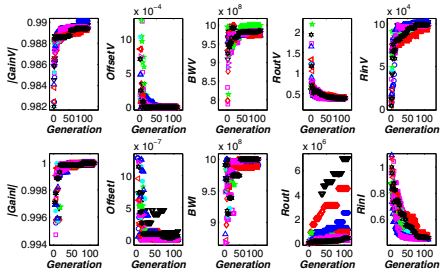

Fig. 4. Generation VS Objectives for MOEA/D for CCII$^+$ Optimization

share the same width) of the circuit, as shown in Table IV. For the second problem, we have 15 variables and 12

TABLE IV
CFOA ENCODING

gene	Design Variable	Encoding Transistors
x_1	L	$M_1, \ldots M_{25}$
x_2	W_1	$M_{11}, M_{12}, M_{13}, M_{14}$
x_3	W_2	M_8, M_9, M_{10}
x_4	W_3	M_6
x_5	W_4	M_7
x_6	W_5	M_1, M_3
x_7	W_6	M_2, M_4
x_8	W_7	M_{15}
x_9	W_8	M_5
x_{10}	W_9	M_{23}, M_{24}
x_{11}	W_{10}	M_{16}, M_{17}
x_{12}	W_{11}	M_{22}, M_{21}
x_{13}	W_{12}	M_{19}, M_{20}
x_{14}	W_{13}	M_{18}
x_{15}	W_{14}	M_{25}

objective functions. The domain for the input variables is $x_1 \in \{0.36\ \mu m, 0.54\ \mu m, 0.72\ \mu m\}$, $x_i \in [0.36\ \mu m, 80\ \mu m]$, for $i \in [2, \ldots, 15]$ and the twelve objectives are:

- $f_1(\mathbf{x}) = 1 -$ (voltage gain); from port Y to port X.
- $f_2(\mathbf{x}) =$ (voltage offset); between port Y and port X.
- $f_3(\mathbf{x}) = 1/$(voltage band width); from port Y to port X.
- $f_4(\mathbf{x}) =$ (output resistance); in port X.
- $f_5(\mathbf{x}) = 1 -$ (current gain); from port X to port Z.
- $f_6(\mathbf{x}) =$ (current offset); between port X and port Z.
- $f_7(\mathbf{x}) = 1/$(current band width); from port X to port Z.
- $f_8(\mathbf{x}) = 1/$(output resistance); in port Z.
- $f_9(\mathbf{x}) = 1 -$ (voltage gain); from port Z to port W.
- $f_{10}(\mathbf{x}) =$ (voltage offset); between port Z and port W.
- $f_{11}(\mathbf{x}) = 1/$(voltage band width); from port Z to port W.
- $f_{12}(\mathbf{x}) =$ (output resistance); in port W.

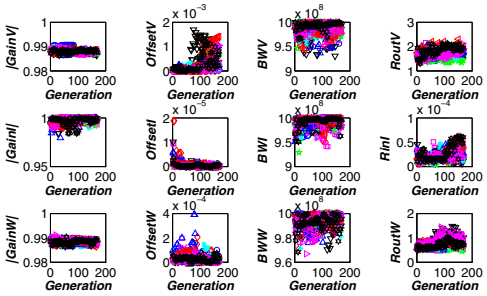

Fig. 5. Generation VS Objectives for NSGA-II for CFOA Optimization

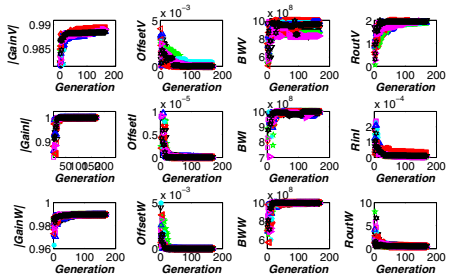

Fig. 6. Generation VS Objectives for MOEA/D for CFOA Optimization

TABLE V
NSGA-II OPTIMIZATION RESULTS FOR THE CFOA

	GainV ($\frac{V}{V}$)	OffsetV (V)	BWV (Hz)	RoutV (Ω)
MAX	0.9880	6.098e-003	6.303e+008	7.7824
MIN	0.9707	4.868e-004	3.190e+008	0.7915
AVG	0.9853	2.495e-003	4.871e+008	1.5373
STD	2.002e-003	8.009e-004	5.247e+007	0.7503
	GainI ($\frac{I}{I}$)	OffsetI (A)	BWI (Hz)	RoutI (Ω)
MAX	0.9986	4.976e-005	9.996e+008	8.646e+004
MIN	0.6017	2.111e-007	1.248e+008	2.760e+003
AVG	0.8513	1.851e-005	8.087e+008	1.581e+004
STD	0.1001	1.350e-005	1.522e+008	9.532e+003
	GainW ($\frac{V}{V}$)	OffsetW (V)	BWW (Hz)	RoutW (Ω)
MAX	0.9890	7.348e-003	9.893e+008	21.2337
MIN	0.9754	7.205e-006	3.219e+008	0.8430
AVG	0.9841	1.744e-003	7.084e+008	3.2157
STD	2.249e-003	1.312e-003	1.186e+008	2.5300

The CFOA was optimized along 168 generations over 10 runs, and the population size for 168 by using DE [12]. Figures 5 and 6 depict the behavior of the best values in each generation of the CFOA for NSGA-II and MOEA/D, respectively. Tables V and VI show the maximum, minimum, average and standard deviation values for NSGA-II and MOEA/D.

C. Discussion of Results

For the CCII$^+$, MOEA/D exhibits the best results for the offset in voltage and current mode, and for the input resistance

TABLE VI
MOEA/D OPTIMIZATION RESULTS FOR THE CFOA

	GainV ($\frac{V}{V}$)	OffsetV (V)	BWV (Hz)	RoutV (Ω)
MAX	0.9893	6.984e-003	6.641e+008	50.2381
MIN	0.9344	1.211e-005	2.268e+008	0.6119
AVG	0.9851	2.236e-003	4.595e+008	1.8835
STD	5.695e-003	1.167e-003	6.571e+007	2.9437
	GainI ($\frac{I}{I}$)	OffsetI (A)	BWI (Hz)	RoutI (Ω)
MAX	1.0000	4.920e-005	9.999e+008	2.809e+005
MIN	0.6022	2.168e-009	1.011e+008	5.708e+003
AVG	0.8997	1.135e-005	7.743e+008	2.535e+004
STD	0.1044	1.061e-005	2.242e+008	2.892e+004
	GainW ($\frac{V}{V}$)	OffsetW (V)	BWW (Hz)	RoutW (Ω)
MAX	0.9899	7.899e-003	9.994e+008	65.7684
MIN	0.9275	7.635e-007	2.730e+008	0.4185
AVG	0.9851	1.573e-003	6.507e+008	3.4540
STD	7.186e-003	1.181e-003	1.659e+008	6.6713

in voltage mode. The improvement is most remarkable (Tables II and III). The average is closer for both methods although the standard deviation is better in NSGA-II than MOEA/D.

For the CFOA, the behavior is similar as for the CCII$^+$, MOEA/D has the best performance (in optimal and average objective values) but only for offset in voltage and current, there is a large improvement. Regarding to the standard deviation, MOEA/D improves its values but for output resistances presents an asymmetric behavior. This time the variables values for both algorithms, changed to handle the large number of objectives and variables.

It can be seen that MOEA/D shows better performance because, besides to find best objectives values than NSGA-II, its diversity feature, tries to explore the whole search space, finding wider range of values in the objectives values compared with NSGA-II. If we compare de MOEA/D average objective values with their standard deviations, it is possible to see how the largest number of solutions are concentred around the average and a little ones are exploring promising areas.

On the one hand, by comparing Fig. 3 with Fig. 4, it is possible to notice that MOEA/D reaches the final value, in less generations than NSGA-II. In the same way, Fig. 5 and Fig. 6 exhibit a similar behavior. On the other hand, by comparing Table II with Table III and Table V with Table VI, NSGA-II has more symmetry in the solutions set and avoids to explore areas which are so far from the objective increasing the ensure to find a solution without the need to make a lot of runs.

V. CONCLUSION

We have shown the behavior of the generations by applying NSGA-II and MOEA/D to size a CCII+ and a CFOA. Both mixed-mode circuits were codified with 9 and 15 variables, respectively, and with 10 and 12 objectives.

In the sizing of the CCII$^+$, the solutions of both MOEAs in the objective space were very close. Although MOEA/D improves its average performance over NSGA-II, this last one exhibited more symmetry denoted by its standard deviation.

In the sizing of the CFOA, MOEA/D had the best performance but only for the offset in voltage and current.

Finally, the behavior of both MOEAs along the generations, showed that MOEA/D has the possibility to reach admissible values in less generations, and NSGA-II has the possibility to improve the results through a higher number of generations. In general, for both mixed-mode circuits, both MOEAs found closer optimized results, in most cases MOEA/D exhibited the best optimal values while NSGA-II exhibited the best symmetry.

VI. ACKNOWLEDGMENTS

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