

The background of the entire page features a light gray circuit board pattern with various lines and circular nodes. On the right side, there is a vertical bar composed of three columns of small, repeating rectangular shapes. The first column is red, the second is yellow, and the third is blue.

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Specification of FDTC TFT-LCD module

FLC48SXC8V-10

Approval
Date :
By :

This Product is designed, developed and manufactured as contemplated for general use, including without limitation, general office use, personal use, household use, and ordinary industrial use, but is not designed, developed and manufactured as contemplated for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (hereinafter "High Safety Required Use"), including without limitation, nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system. Fujitsu shall not be liable against the Customer and/or any third party for any claims or damages arising in connection with the High Safety Required Use of the Product without permission.

Specification No. : Tech Bes LCD-00157

Issue Date : May 13, 2003

Issued by : Katewori Tanaka

K. Tanaka

Director

Design Dept., Technology Div.

FUJITSU DISPLAY TECHNOLOGIES CORPORATION

REVISION HISTORY

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Revision	Date	Prepared	Checked		Approved	Summary
01A	Aug. 30,2002	T.Ito	T. Ito		K.Tanaka	1st issue
02A	Mar. 07,2003	M.Hirosawa	T. Ito		K.Tanaka	Change Back Light
03A	Apr.10,2003	T. Ito	T.Ito		K.Tanaka	Change L2,L13 resistor 0Ω to 22Ω.
04A	Apr.10,2003	T. Ito	T.Ito		K.Tanaka	Change LVDS Receiver NS to Thine.

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05	20030307	E.Nitto	T.Ito	K.Tanaka	Revised P.35,36				TITLE					FLC48SXC8V-10					
08	20030513	T. Ito		K.Tanaka	Revised P19,28,35				DRAW. NO.					CUST.					
07	20030410	T.Ito		K.Tanaka	Add 03A,04A, Revised P7,13,14,26				Tech Bes LCD-00157										
06	20030329	T. Ito		K.Tanaka	Revised P35														
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION				FUJITSU DISPLAY TECHNOLOGIES					SITE	1 / 36				
	DESIG.	20020830	T.Ito	CHECK	E.Nitto	K Nukiyama	APPR.	K.Tanaka	CORPORATION										

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6. ABSOLUTE MAXIMUM RATING

Table 6-1 shows the absolute maximum rating of this LCD module.

Table 6-1 Absolute Maximum Rating

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V _{CC}	Ta=25°C	−0.3	—	6.0	V
Input Signal Voltage (LVDS signal, PD,SEL LVDS)	V _{IN}	Ta=25°C	−0.3	—	3.6	V

7. RECOMMENDED OPERATING CONDITIONS

Table 7-1 shows the recommended operating conditions of this LCD module.

Table 7-1 Recommended Operating Conditions

Item		Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage(Logic)		V _{CC}	4.75	—	5.25	V
Ripple Voltage	V _{CC}	V _{RP}	—	—	0.1	V

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						DRAW. NO. Tech Bes LCD-00157							CUST.			
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8. ELECTRICAL SPECIFICATIONS Table 8-1 shows the electrical specifications of this LCD module. Figure 8-1 shows the measurement circuit. Figure 8-2(A) shows the equivalent circuit of the logic signal input area. Figure 8-2(B) shows the equivalent circuit of the supply voltage Input area. ② Table 8-1 Electrical Specifications <table><tr><th>Item</th><th>Symbol</th><th>Condition</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th><th>Remark</th></tr><tr><td>Differential-input Voltage (Hign)</td><td>V_{IH}</td><td rowspan="2">V_{CM}=+1.2V</td><td>—</td><td>—</td><td>100</td><td>mV</td><td></td></tr><tr><td>Differential-input Voltage (Low)</td><td>V_{IL}</td><td>−100</td><td>—</td><td>—</td><td>mV</td><td></td></tr><tr><td>Input Voltage (High)</td><td>V_{IH}</td><td rowspan="5">V_{CC}=+5.0±0.25V V_{SS}=0V DCLK=54MHz Ta=25° C</td><td>2.0</td><td>—</td><td>3.3</td><td>V</td><td rowspan="2">PD SEL LVDS</td></tr><tr><td>Input Voltage (Low)</td><td>V_{IL}</td><td>0</td><td>—</td><td>0.8</td><td>V</td></tr><tr><td>Supply Current</td><td>I_{CC}</td><td>—</td><td>700 800</td><td>1500</td><td>mA</td><td>*1 ③</td></tr><tr><td>Supply Rush Current</td><td>I_{SCC}</td><td>—</td><td>—</td><td>3.5</td><td>A</td><td rowspan="2">*2 ③</td></tr><tr><td>Supply Rush Current Duration(1.5A excess)</td><td>T_{SCC}</td><td>—</td><td>—</td><td>1.0</td><td>ms</td></tr><tr><td rowspan="4">BACK LIGHT(*3)</td><td rowspan="2">CCFL Turn on Voltage</td><td rowspan="2">V_S</td><td>f_L=50kHz,Ta=25°C</td><td>—</td><td>1400</td><td>1600</td><td rowspan="2">V_{rms}</td><td></td></tr><tr><td>f_L=50kHz,Ta=0°C</td><td>—</td><td>1500</td><td>1600</td><td>④</td></tr><tr><td>Lighting Voltage</td><td>V_L</td><td>f_L=50kHz I_L=7mA</td><td>—</td><td>750</td><td>—</td><td>V_{rms}</td><td></td></tr><tr><td>Lighting Frequency</td><td>f_L</td><td>V_L=750V_{rms}</td><td>40</td><td>50</td><td>60</td><td>kHz</td><td></td></tr><tr><td></td><td>Tube Current</td><td>I_L</td><td>f_L=50kHz V_L=750V_{rms}</td><td>4</td><td>7</td><td>8</td><td>mArms</td><td>*4</td></tr></table> (*1) Typical current situation : Color bar pattern. Vcc=5.0V Maximum current situation : White pattern. Vcc=4.75V Without rush current. (*2) These items prescribe the rush current for starting internal DC/DC. Charging current to capacitors of Vcc is not prescribed. (*3) Back-light specifications are valid when using a suitable inverter such as the FLCV-13 (*4) Tube current (I_L) shows the value of the current that is consumed at one lamp. This LCD module has 4 lamps. Each 2 lamps are placed at upper side and lower side of the display. 2 lamps is connected in parallel. Each low voltage terminals are connected with separate cable to Back-light connector. <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">TITLE FLC48SXC8V-10</td></tr><tr><td>04</td><td>20030128</td><td></td><td></td><td></td><td>Add Typ. Vs spec. at 0°C.</td><td colspan="2">DRAW. NO.</td></tr><tr><td>03</td><td>20021206</td><td></td><td></td><td></td><td>Change current spec.</td><td colspan="2">Tech Bes LCD-00157</td></tr><tr><td>02</td><td>20021101</td><td></td><td></td><td></td><td>Change electrical spec.</td><td colspan="2">CUST.</td></tr><tr><td>EDIT</td><td>DATE</td><td>DESIG.</td><td>CHECK</td><td>APPR.</td><td colspan="2">DESCRIPTION</td><td rowspan="2">FUJITSU DISPLAY TECHNOLOGIES CORPORATION</td></tr><tr><td>DESIG.</td><td></td><td></td><td>CHECK</td><td></td><td>APPR.</td><td></td></tr></table> 1								Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remark	Differential-input Voltage (Hign)	V _{IH}	V _{CM} =+1.2V	—	—	100	mV		Differential-input Voltage (Low)	V _{IL}	−100	—	—	mV		Input Voltage (High)	V _{IH}	V _{CC} =+5.0±0.25V V _{SS} =0V DCLK=54MHz Ta=25° C	2.0	—	3.3	V	PD SEL LVDS	Input Voltage (Low)	V _{IL}	0	—	0.8	V	Supply Current	I _{CC}	—	700 800	1500	mA	*1 ③	Supply Rush Current	I _{SCC}	—	—	3.5	A	*2 ③	Supply Rush Current Duration(1.5A excess)	T _{SCC}	—	—	1.0	ms	BACK LIGHT(*3)	CCFL Turn on Voltage	V _S	f _L =50kHz,Ta=25°C	—	1400	1600	V _{rms}		f _L =50kHz,Ta=0°C	—	1500	1600	④	Lighting Voltage	V _L	f _L =50kHz I _L =7mA	—	750	—	V _{rms}		Lighting Frequency	f _L	V _L =750V _{rms}	40	50	60	kHz			Tube Current	I _L	f _L =50kHz V _L =750V _{rms}	4	7	8	mArms	*4							TITLE FLC48SXC8V-10		04	20030128				Add Typ. Vs spec. at 0°C.	DRAW. NO.		03	20021206				Change current spec.	Tech Bes LCD-00157		02	20021101				Change electrical spec.	CUST.		EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION		FUJITSU DISPLAY TECHNOLOGIES CORPORATION	DESIG.			CHECK		APPR.		A		B		C		D		E		F	
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Supply Current	I _{CC}		—	700 800	1500	mA	*1 ③																																																																																																																																																											
Supply Rush Current	I _{SCC}		—	—	3.5	A	*2 ③																																																																																																																																																											
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Measurement circuit is based on Figure 8-1.

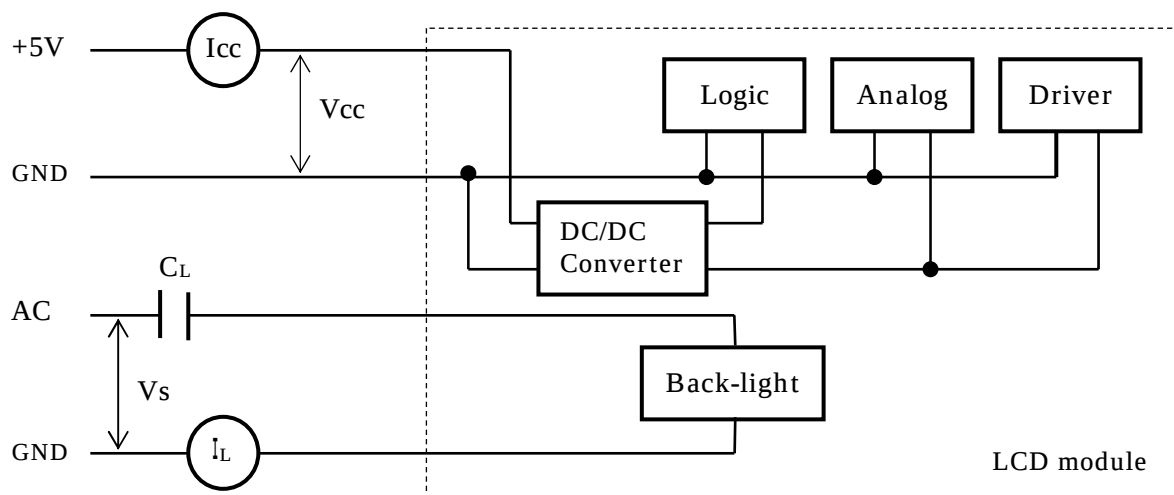
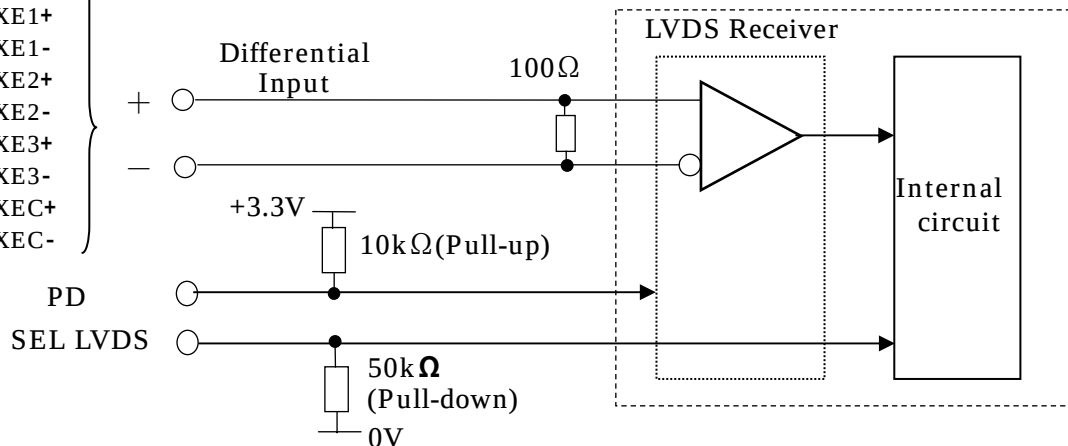


Figure 8-1 Measurement circuit

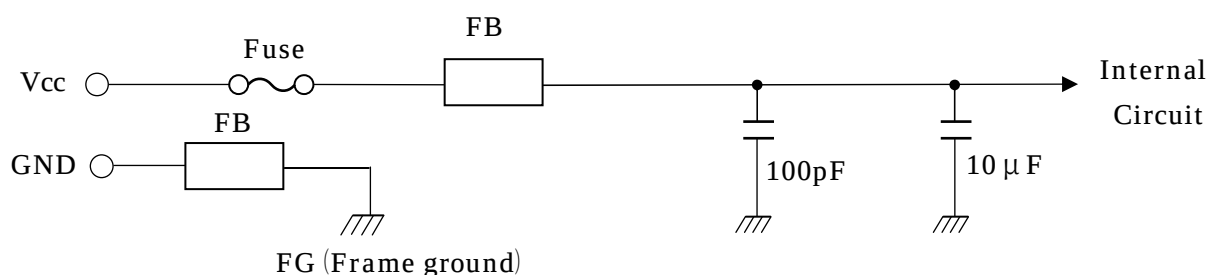
Input signals (LVDS Dual)

RX00+ RXE0+
RX00- RXE0-
RX01+ RXE1+
RX01- RXE1-
RX02+ RXE2+
RX02- RXE2-
RX03+ RXE3+
RX03- RXE3-
RXOC+ RXEC+
RXOC- RXEC-



⑦LVDS Receiver : DS90CF386 (National Semiconductor Corp. or equivalent)
TH63LVDF84 (Thine)

Figure 8-2(A) Equivalent circuit of logic signal Input



Fuse : F0603C3R00FWTRM 3.0A (Kyocera Corp. or equivalent)

② FB : Ferrite Bead

Figure 8-2(B) Equivalent circuit of power supply

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07	20030410					Change LVDS Receiver.					DRAW. NO.		CUST.	
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Ta=25°C, Signal Timing=Typ.

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Based on Figure 9-1.

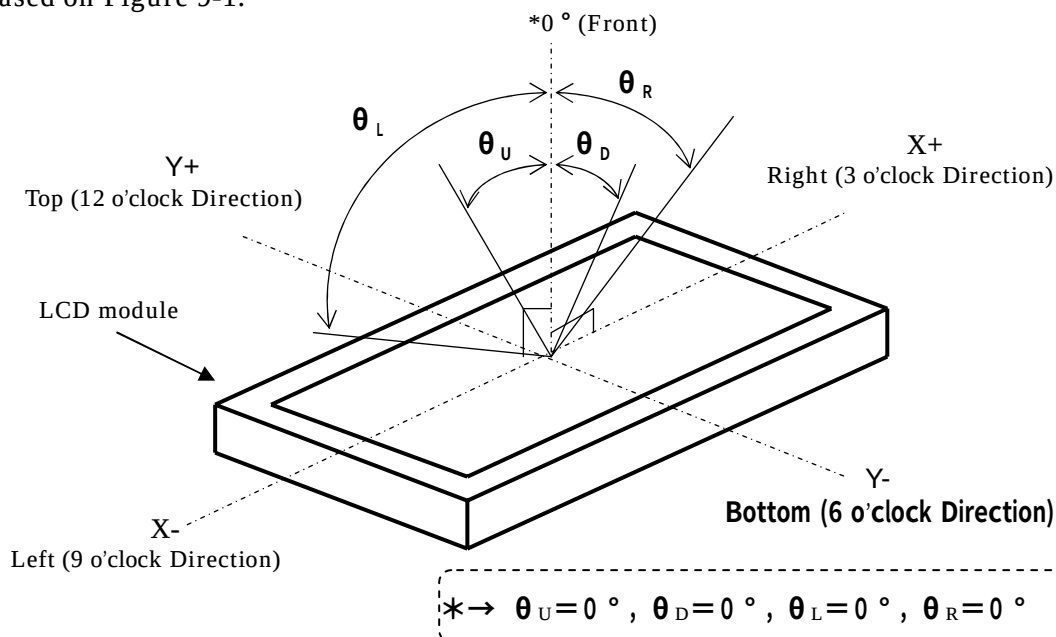


Figure 9-1 Definition of Viewing Angle (1)

Note 2) Definition of Viewing Angle (2)

Based on Figure 9-2.

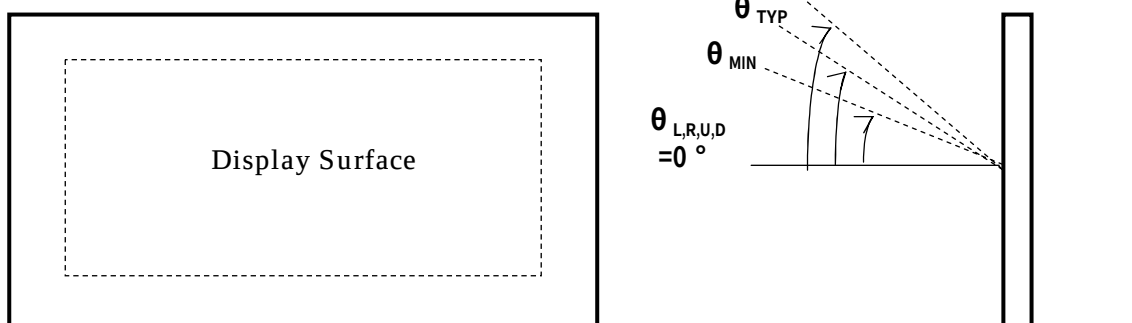


Figure 9-2 Definition of Viewing Angle (2)

Note 3) Definition of Contrast Ratio (CR)

Determined by Formula (1) based on Figure 9-3 Voltage-Brightness characteristics. B

$$= \frac{L_W(\text{Brightness at white})}{L_B(\text{Brightness at black})} \dots\dots(1)$$

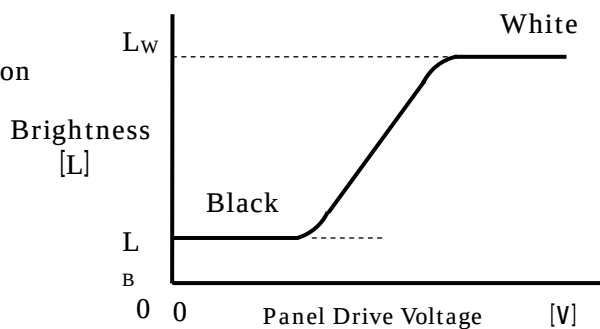


Figure 9-3 Voltage-Brightness Characteristics

Note 3) Definition of Contrast Ratio (CR)
Determined by Formula (1) based on Figure 9-3 Voltage-Brightness characteristics.

$$= \frac{L_w (\text{Brightness at white})}{L_b (\text{Brightness at black})} \cdots \cdots (1)$$

Figure 9-3 Voltage-Brightness Characteristics

Based on Figure 9-4.

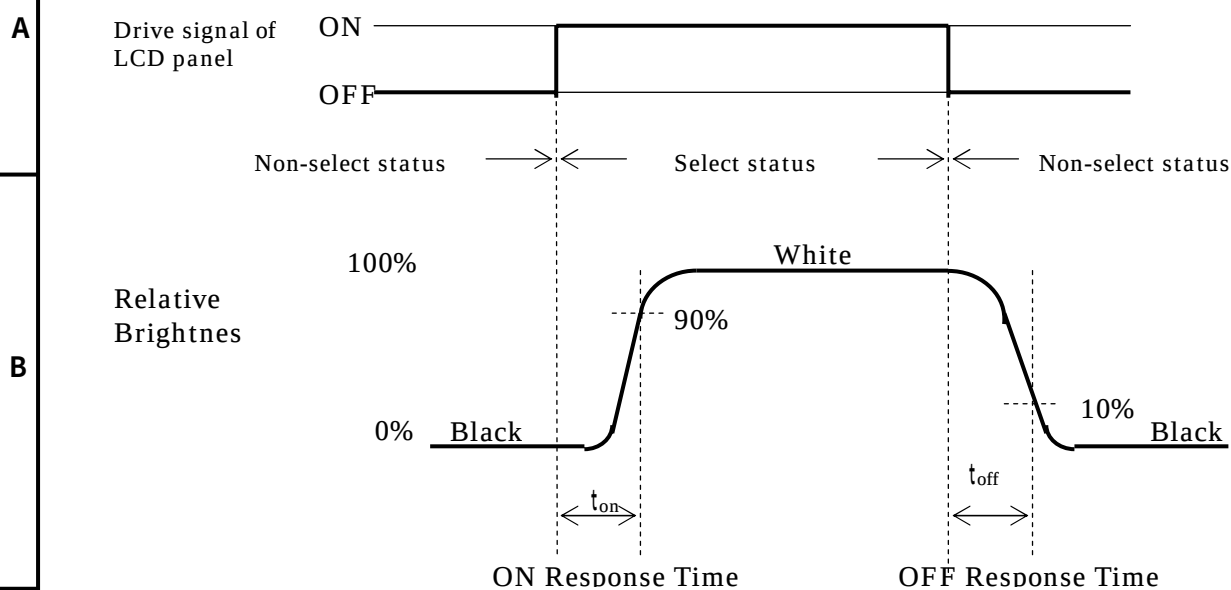


Figure 9-4 Definition of Response Time

Note 5) Contrast Ratio and Response Measurement System

Based on Figure 9-5.

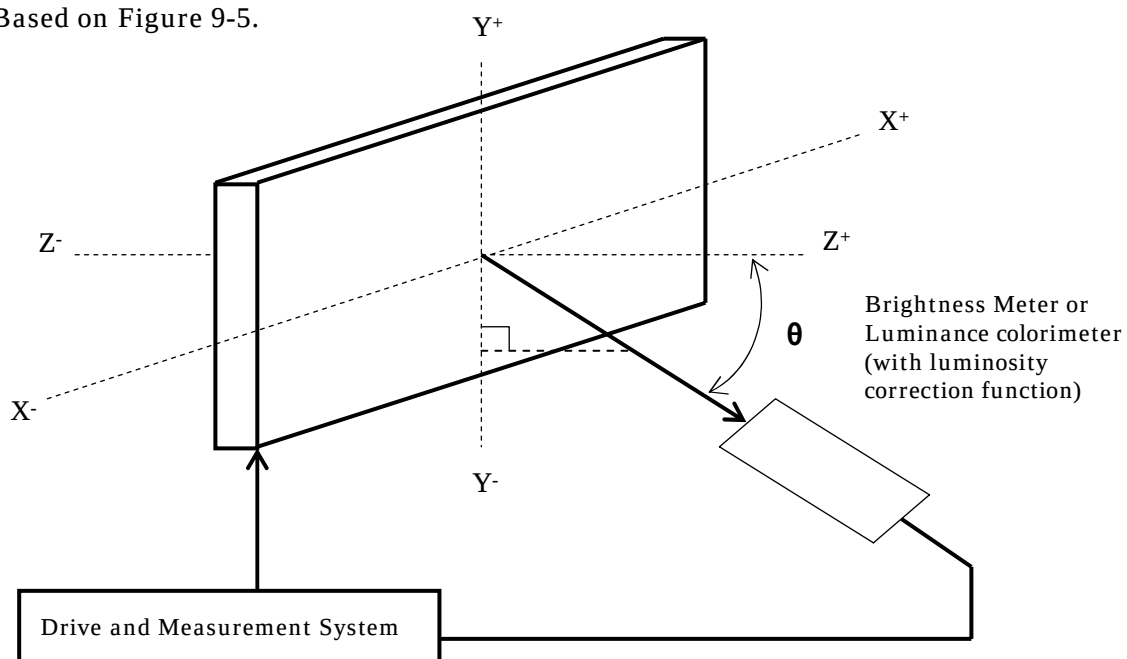


Figure 9-5 Contrast Ratio and Response Time Measurement System

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10-1 Signal descriptions

Table 10-1 shows the description and configuration of interface signals (CN1).

Table 10-1 Interface signals (CN1)

Pin No.	Symbol	I/O	Function
1	RxO0-	I	Negative differential input
2	RxO0+	I	Positive differential input
3	RxO1-	I	Negative differential input
4	RxO1+	I	Positive differential input
5	RxO2-	I	Negative differential input
6	RxO2+	I	Positive differential input
7	GND	—	Ground
8	RxOC-	I	Negative differential input
9	RxOC+	I	Positive differential input
10	RxO3-	I	Negative differential input
11	RxO3+	I	Positive differential input
12	RxE0-	I	Negative differential input
13	RxE0+	I	Positive differential input
14	GND	—	Ground
15	RxE1-	I	Negative differential input
16	RxE1+	I	Positive differential input
17	GND	—	Ground
18	RxE2-	I	Negative differential input
19	RxE2+	I	Positive differential input
20	RxEC-	I	Negative differential input
21	RxEC+	I	Positive differential input
22	RxE3-	I	Negative differential input
23	RxE3+	I	Positive differential input
24	GND	—	Ground
25	SEL LVDS	I	Select LVDS Mapping
26	PD	—	LVDS Core Power Down
27	TST	—	Test pin *1
28	Vcc	—	+5V power supply
29	Vcc	—	+5V power supply
30	Vcc	—	+5V power supply

User's connector : FI-X30M (FPC type) (Japan Aviation Electronics)

FI-X30H (Wire type)

FI-X30C (Coaxial cable type)

*1: Keep open. (Internal test use only.)

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Table 10-2A LVDS Data Assignment (SEL LVDS = L)

Input odd or even data depending on the display position of the LCD module.

						TITLE										
						FLC48SXC8V-10										
						DRAW. NO.										
						CUST.										
07	20030410				Change LVDS Receiver.					Tech Bes LCD-00157						
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1		2		3		4						
Table 10-2B LVDS Data Assignment (SEL LVDS = H)												
A	Input signal *1		Transmitter DS90CF383,C385		Interface connector		⑦Receiver DS90CF386, THC63LVDF84		LCD Control input			
			pin	INPUT	System side	LCD module pin	pin	OUTPUT				
	B	LVDS Odd	RO0	51	TxIN0	Tx OUT0+	2	RxO0+	27	RxOUT0	RO0	
RO1			52	TxIN1	29				RxOUT1	RO1		
RO2			54	TxIN2	30				RxOUT2	RO2		
RO3			55	TxIN3	32				RxOUT3	RO3		
RO4			56	TxIN4	33				RxOUT4	RO4		
RO5			3	TxIN6	Tx OUT0-	1	RxO0-	35	RxOUT6	RO5		
GO0			4	TxIN7				37	RxOUT7	GO0		
GO1			6	TxIN8				38	RxOUT8	GO1		
GO2			7	TxIN9				39	RxOUT9	GO2		
GO3			11	TxIN12	Tx OUT1+	4	RxO1+	43	RxOUT12	GO3		
GO4			12	TxIN13				45	RxOUT13	GO4		
GO5			14	TxIN14				46	RxOUT14	GO5		
BO0			15	TxIN15				47	RxOUT15	BO0		
BO1			19	TxIN18				51	RxOUT18	BO1		
BO2			20	TxIN19	Tx OUT1-	3	RxO1-	53	RxOUT19	BO2		
BO3			22	TxIN20				54	RxOUT20	BO3		
BO4			23	TxIN21				55	RxOUT21	BO4		
BO5			24	TxIN22				1	RxOUT22	BO5		
RSVD			27	TxIN24				3	RxOUT24	Not use		
RSVD			28	TxIN25	Tx OUT2+	6	RxO2+	5	RxOUT25	Not use		
ENAB			30	TxIN26				6	RxOUT26	ENAB		
RO6			50	TxIN27				7	RxOUT27	RO6		
RO7			2	TxIN5				34	RxOUT5	RO7		
GO6			8	TxIN10	Tx OUT2-	5	RxO2-	41	RxOUT10	GO6		
GO7			10	TxIN11				42	RxOUT11	GO7		
BO6			16	TxIN16				49	RxOUT16	BO6		
BO7			18	TxIN17				50	RxOUT17	BO7		
RSVD			25	TxIN23				2	RxOUT23	Not use		
C			LVDS Even	DCLK	31	TxCLK IN	TxCLK OUT+	9	RxCLK IN+	26	RxCLK OUT	DCLK
							TxCLK OUT-	8	RxCLK IN-			
	RE0	51		TxIN0	Tx OUT0+	13	RxEO+	27	RxOUT0	RE0		
	RE1	52		TxIN1				29	RxOUT1	RE1		
	RE2	54		TxIN2				30	RxOUT2	RE2		
	RE3	55		TxIN3				32	RxOUT3	RE3		
	RE4	56		TxIN4				33	RxOUT4	RE4		
	RE5	3		TxIN6	Tx OUT0-	12	RxEO-	35	RxOUT6	RE5		
	GE0	4		TxIN7				37	RxOUT7	GE0		
	GE1	6		TxIN8				38	RxOUT8	GE1		
	GE2	7		TxIN9				39	RxOUT9	GE2		
	GE3	11		TxIN12	Tx OUT1+	16	RxE1+	43	RxOUT12	GE3		
	GE4	12		TxIN13				45	RxOUT13	GE4		
	GE5	14		TxIN14				46	RxOUT14	GE5		
	BE0	15		TxIN15				47	RxOUT15	BE0		
	BE1	19		TxIN18				51	RxOUT18	BE1		
	BE2	20		TxIN19	Tx OUT1-	15	RxE1-	53	RxOUT19	BE2		
	BE3	22		TxIN20				54	RxOUT20	BE3		
	BE4	23		TxIN21				55	RxOUT21	BE4		
	BE5	24		TxIN22				1	RxOUT22	BE5		
	RSVD	27		TxIN24				3	RxOUT24	Not use		
	RSVD	28		TxIN25	Tx OUT2+	19	RxEO2+	5	RxOUT25	Not use		
	RSVD	30		TxIN26				6	RxOUT26	Not use		
	RE6	50		TxIN27				7	RxOUT27	RE6		
	RE7	2		TxIN5				34	RxOUT5	RE7		
	GE6	8		TxIN10	Tx OUT2-	18	RxE2-	41	RxOUT10	GE6		
	GE7	10		TxIN11				42	RxOUT11	GE7		
	BE6	16		TxIN16				49	RxOUT16	BE6		
	BE7	18		TxIN17				50	RxOUT17	BE7		
	RSVD	25		TxIN23				2	RxOUT23	Not use		
D	LVDS Even	DCLK	31	TxCLK IN	TxCLK OUT+	21	RxCLK IN+	26	RxCLK OUT	Not use		
					TxCLK OUT-	20	RxCLK IN-					
		RE0	51	TxIN0	Tx OUT0+	13	RxEO+	27	RxOUT0	RE0		
		RE1	52	TxIN1				29	RxOUT1	RE1		
		RE2	54	TxIN2				30	RxOUT2	RE2		
		RE3	55	TxIN3				32	RxOUT3	RE3		
		RE4	56	TxIN4				33	RxOUT4	RE4		
		RE5	3	TxIN6	Tx OUT0-	12	RxEO-	35	RxOUT6	RE5		
		GE0	4	TxIN7				37	RxOUT7	GE0		
		GE1	6	TxIN8				38	RxOUT8	GE1		
		GE2	7	TxIN9				39	RxOUT9	GE2		
		GE3	11	TxIN12	Tx OUT1+	16	RxE1+	43	RxOUT12	GE3		
		GE4	12	TxIN13				45	RxOUT13	GE4		
		GE5	14	TxIN14				46	RxOUT14	GE5		
		BE0	15	TxIN15				47	RxOUT15	BE0		
		BE1	19	TxIN18				51	RxOUT18	BE1		
		BE2	20	TxIN19	Tx OUT1-	15	RxE1-	53	RxOUT19	BE2		
		BE3	22	TxIN20				54	RxOUT20	BE3		
		BE4	23	TxIN21				55	RxOUT21	BE4		
		BE5	24	TxIN22				1	RxOUT22	BE5		
		RSVD	27	TxIN24				3	RxOUT24	Not use		
		RSVD	28	TxIN25	Tx OUT2+	19	RxE2+	5	RxOUT25	Not use		
		RSVD	30	TxIN26				6	RxOUT26	Not use		
		RE6	50	TxIN27				7	RxOUT27	RE6		
		RE7	2	TxIN5				34	RxOUT5	RE7		
		GE6	8	TxIN10	Tx OUT2-	18	RxE2-	41	RxOUT10	GE6		
		GE7	10	TxIN11				42	RxOUT11	GE7		
		BE6	16	TxIN16				49	RxOUT16	BE6		
		BE7	18	TxIN17				50	RxOUT17	BE7		
		RSVD	25	TxIN23				2	RxOUT23	Not use		
E	LVDS Even	DCLK	31	TxCLK IN	TxCLK OUT+	21	RxCLK IN+	26	RxCLK OUT	Not use		
					TxCLK OUT-	20	RxCLK IN-					
		RE0	51	TxIN0	Tx OUT0+	13	RxEO+	27	RxOUT0	RE0		
		RE1	52	TxIN1				29	RxOUT1	RE1		
		RE2	54	TxIN2				30	RxOUT2	RE2		
		RE3	55	TxIN3				32	RxOUT3	RE3		
		RE4	56	TxIN4				33	RxOUT4	RE4		
		RE5	3	TxIN6	Tx OUT0-	12	RxEO-	35	RxOUT6	RE5		
		GE0	4	TxIN7				37	RxOUT7	GE0		
		GE1	6	TxIN8				38	RxOUT8	GE1		
		GE2	7	TxIN9				39	RxOUT9	GE2		
		GE3	11	TxIN12	Tx OUT1+	16	RxE1+	43	RxOUT12	GE3		
		GE4	12	TxIN13				45	RxOUT13	GE4		
		GE5	14	TxIN14				46	RxOUT14	GE5		
		BE0	15	TxIN15				47	RxOUT15	BE0		
		BE1	19	TxIN18				51	RxOUT18	BE1		
		BE2	20	TxIN19	Tx OUT1-	15	RxE1-	53	RxOUT19	BE2		
		BE3	22	TxIN20				54	RxOUT20	BE3		
		BE4	23	TxIN21				55	RxOUT21	BE4		
		BE5	24	TxIN22				1	RxOUT22	BE5		
		RSVD	27	TxIN24				3	RxOUT24	Not use		
		RSVD	28	TxIN25	Tx OUT2+	19	RxE2+	5	RxOUT25	Not use		
		RSVD	30	TxIN26				6	RxOUT26	Not use		
		RE6	50	TxIN27				7	RxOUT27	RE6		
		RE7	2	TxIN5				34	RxOUT5	RE7		
		GE6	8	TxIN10	Tx OUT2-	18	RxE2-	41	RxOUT10	GE6		
		GE7	10	TxIN11				42	RxOUT11	GE7		
		BE6	16	TxIN16				49	RxOUT16	BE6		
		BE7	18	TxIN17				50	RxOUT17	BE7		
		RSVD	25	TxIN23				2	RxOUT23	Not use		
F	LVDS Even	DCLK	31	TxCLK IN	TxCLK OUT+	21	RxCLK IN+	26	RxCLK OUT	Not use		
					TxCLK OUT-	20	RxCLK IN-					
		RE0	51	TxIN0	Tx OUT0+	13	RxEO+	27	RxOUT0	RE0		
		RE1	52	TxIN1				29	RxOUT1	RE1		
		RE2	54	TxIN2				30	RxOUT2	RE2		
		RE3	55	TxIN3				32	RxOUT3	RE3		
		RE4	56	TxIN4				33	RxOUT4	RE4		
		RE5	3	TxIN6	Tx OUT0-	12	RxEO-	35	RxOUT6	RE5		
		GE0	4	TxIN7				37	RxOUT7	GE0		
		GE1	6	TxIN8				38	RxOUT8	GE1		
		GE2	7	TxIN9				39	RxOUT9	GE2		
		GE3	11	TxIN12	Tx OUT1+	16	RxE1+	43	RxOUT12	GE3		
		GE4	12	TxIN13				45	RxOUT13	GE4		
		GE5	14	TxIN14				46	RxOUT14	GE5		
		BE0	15	TxIN15				47	RxOUT15	BE0		
		BE1	19	TxIN18				51	RxOUT18	BE1		
		BE2	20	TxIN19	Tx OUT1-	15	RxE1-	53	RxOUT19	BE2		
		BE3	22	TxIN20				54	RxOUT20	BE3		
		BE4	23	TxIN21				55	RxOUT21	BE4		
		BE5	24	TxIN22				1	RxOUT22	BE5		
		RSVD	27	TxIN24				3	RxOUT24	Not use		
		RSVD	28	TxIN25	Tx OUT2+	19	RxE2+	5	RxOUT25	Not use		
		RSVD	30	TxIN26				6	RxOUT26	Not use		
		RE6	50	TxIN27				7	RxOUT27	RE6		
		RE7	2	TxIN5				34	RxOUT5	RE7		
		GE6	8	TxIN10	Tx OUT2-	18	RxE2-	41	RxOUT10	GE6		
		GE7	10	TxIN11				42	RxOUT11	GE7		
		BE6	16	TxIN16				49	RxOUT16	BE6		
		BE7	18	TxIN17				50	RxOUT17	BE7		
		RSVD	25	TxIN23				2	RxOUT23	Not use		
*1 ·RSVD (reserved) pin on a transmitter should be connected with Ground.												
·Input odd or even data depending on the display position of the LCD module.												
TITLE FLC48SXC8V-10												
DRAW. NO. Tech Bes LCD-00157												
CUST.												
07 20030410 Change LVDS Receiver.												
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Table 10-3 shows the Color Data Assignment.

Color			R Input data								G Input data								B Input data							
	Odd Even		R7 R6 R5 R4 R3 R2 R1 R0	R7 R6 R5 R4 R3 R2 R1 R0	G7 G6 G5 G4 G3 G2 G1 G0	G7 G6 G5 G4 G3 G2 G1 G0	B7 B6 B5 B4 B3 B2 B1 B0	B7 B6 B5 B4 B3 B2 B1 B0																		
Basic Color	Black		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	Blue		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																			
	Green		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	Cyan		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																			
	Red		1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	Magenta		1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																			
	Yellow		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	White		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																			
Red	Black	0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	⬆	1	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
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	Brighter	253	1 1 1 1 1 1 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	⬇	254	1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
Red	255	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																				
Green	Black	0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	⬆	1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
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	⬇	:	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :																			
	Brighter	253	0 0 0 0 0 0 0 0	1 1 1 1 1 1 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	⬇	254	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
Green	255	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																				
Blue	Black	0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0																			
	⬆	1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1																			
	⬆	:	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :																			
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	⬇	:	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :	: : : : ~ : :																			
	Brighter	253	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 0 1	1 1 1 1 1 1 0 1																			
	⬇	254	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 0	1 1 1 1 1 1 1 0																			
Blue	255	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1																				

Larger number means brighter level.

Note.2) Data; 1=High, 0=Low

Note 3) Color data consist of 8 bit red, green and blue data of odd and even number pixel data. Total data number is 48 signals. This module is able to display 16,777,216 colors because each red, green and blue data is controlled independently.

DATE	DOCUMENT CONTROL SECTION

						TITLE FLC48SXC8V-10							
						DRAW. NO. Tech Bes LCD-00157							CUST.
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION							FUJITSU DISPLAY TECHNOLOGIES CORPORATION	SHEET 15/
	DESIG.			CHECK			APPR.						

1		2		3		4	
10-4 Input Signal Timing							
② Table 10-4 and Figure 10-1 shows the Input Signal Timing at LVDS transmitter.							
Table 10-4 Timing Characteristics (Ta=0~50'C, Vcc=5±0.25V)							
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK signal (Clock)	Period	Tc	16.0	18.5	25.0	ns	
	Frequency	1/Tc	40	54	62.5	MHz	
	Duty	Tch/Tc	45	50	55	%	
	High time	TclkH	5.0	—	—	ns	
	Low time	TclkL	5.0	—	—	ns	
DCLK-Data Timing	Setup time	Tset	3	—	—	ns	
	Hold time	Thold	5	—	—	ns	
ENAB signal	Horizontal Period(1)	Th	5350/Tc+435	844	887 *1	DCLK	Tc=ns
	Horizontal Period(2)	Th	648	—	1023	DCLK	*4
	Hor. Display period	Thd	640	640	640	DCLK	*2
	Vertical Period	Tv	1028 *1	1066	1088 *1	Th	16.67ms
	Ver. Frequency	1/Tv	50	60	76.2	Hz	
	Ver. Display period	Tvd	1024	1024	1024	Th	*2
Data-ENAB timing	Tdn	—	0	—	DCLK	*3	
*1)•horizontal display position is specified by the rise of ENAB. The data latched at falling edge of DCLK after rise of ENAB is displayed at the left edge of the display area. •Vertical display position is specified by the rise of ENAB after low level continuation over 2048 DCLK. The data latched at the rise of ENAB is displayed at the top line of the display area. *2)•If the “High” level period of ENAB is less than 640 DCLK or the number of ENAB in a frame period (Tv) is less than 1024, black color is displayed at the rest of the display area. *3)•If ENAB does not synchronize with the effective display data, the display position does not fit to the display area. *4)•Hor. Period (2) shows the operating range where internal circuit can work correctly. •When ENAB signal is out of Hor. Period (1), the display quality may deteriorate.							
DOCUMENT CONTROL SECTION							
DATE							
						TITLE FLC48SXC8V-10	
						DRAW. NO.	
						Tech Bes LCD-00157	
02 20021101						CUST.	
						Change timing characteristics.	
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION		
DESIG.				CHECK	FUJITSU DISPLAY TECHNOLOGIES CORPORATION		
1						16/	

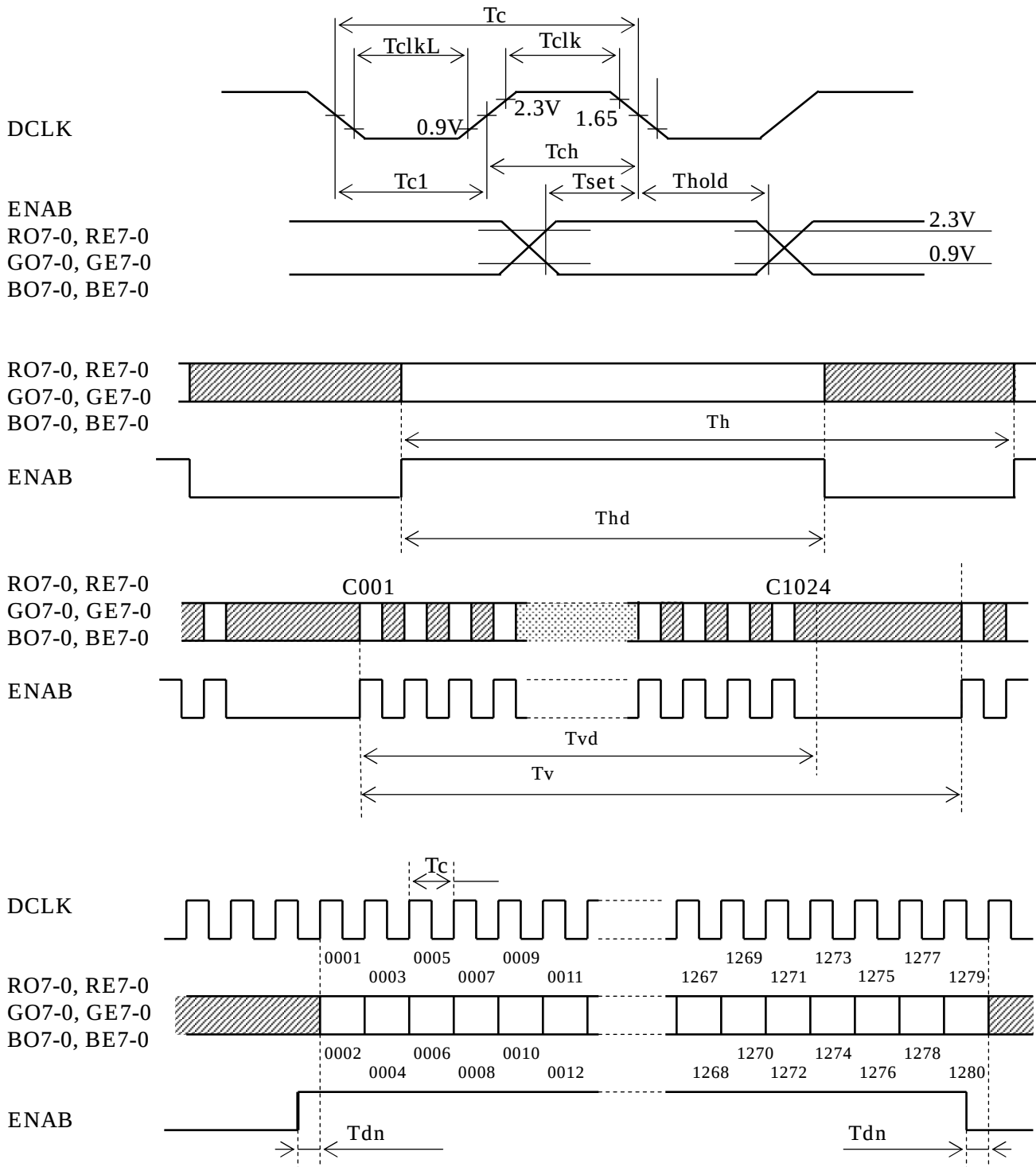


Figure 10-1 Input Signal Timing Chart

						TITLE FLC48SXC8V-10							
						DRAW. NO. Tech Bes LCD-00157						CUST.	
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION					FUJITSU DISPLAY TECHNOLOGIES CORPORATION		Sheet 17 /	
	DESIG.			CHECK			APPR.						

10-4 Correspondence between Data and Display Position

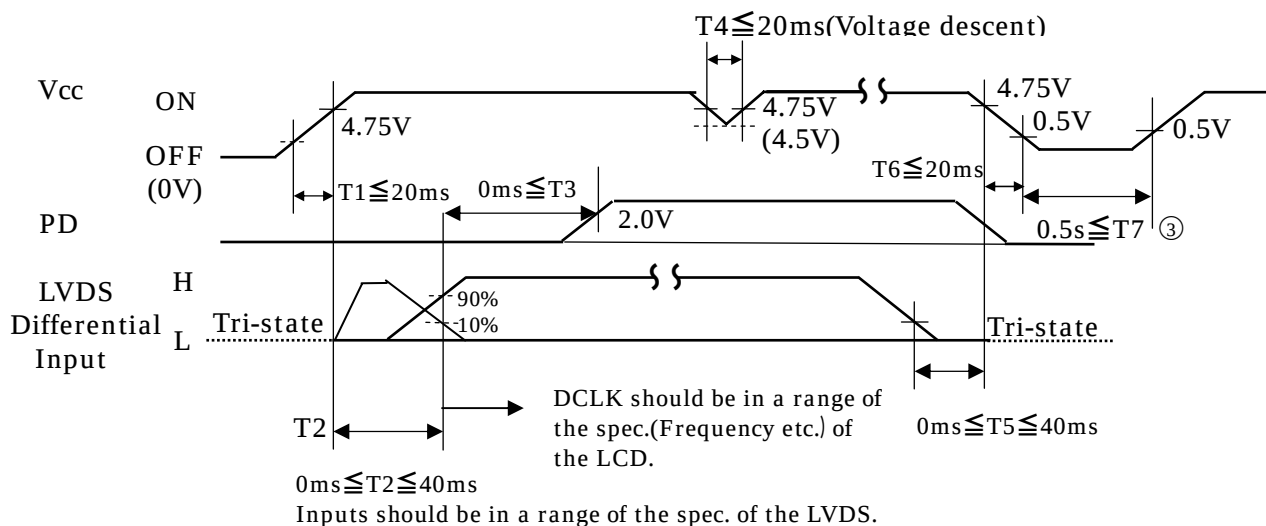
Figure 10-2 shows the Correspondence between Data and Display Position.

	S0001	S0002	S0003	S0004	S0005	S0006	S0007	-----		S3839	S3840	
C001	RO 0001	GO 0001	BO 0001	RE 0002	GE 0002	BE 0002	RO 0003	GO 0003			GE 1280	BE 1280

Figure 10-2 Correspondence Data and Display Position

10-5 Power Supply Sequence

The sequence of input signals and On/Off of the power supply of this LCD module should be in the specification shown in Figure 10-3 to prevent latch-up of the driver ICs and DC driving of the LCD panel.



*Note : PD input can be set open, if it is not used.

Figure 10-3 Power Supply Sequence

DOCUMENT CONTROL SECTION

DATE

						TITLE	FLC48SXC8V-10			
						DRAW. NO.	Tech Bes LCD-00157			
03	20021206					Change T7 timing.			CUST.	
EDIT	DATE	DESIG.	CHECK	APPR.		DESCRIPTION	FUJITSU DISPLAY TECHNOLOGIES CORPORATION			
	DESIG.			CHECK		APPR.			18 /	

A

A

B

B

C

C

D

D

E

- F

						TITLE FLC48SXC8V-10						
08	20030513				Correction of lamp No.	DRAW. NO. Tech Bes LCD-00157					CUST.	
03	20021206				Change calbe color							
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION					FUJITSU DISPLAY TECHNOLOGIES CORPORATION		19/
	DESIG.			CHECK			APPR.					

12-1 Appearance

D:Average diameter [mm], W:Width [mm], L:Length [mm], S=(bright spot size)/(dot size)

						TITLE FLC48SXC8V-10							
						DRAW. NO. Tech Bes LCD-00157						CUST.	
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION					FUJITSU DISPLAY TECHNOLOGIES CORPORATION		SHEET	20 /
	DESIG.			CHECK			APPR.						

		1			2			3			4		
DOCUMENT CONTROL SECTION	DATE	12-2 Dot defects (Bright spots, Dark spots) A <u>12-2-1 Zone</u> · Inside display dot area (376.32×301.056mm) · Display dot area means active area. · One pixel consists of 3 dots (red, green and blue). · Foreign particle and scratch unharmed to display image, such as the foreign particle under polarizer film but outside of the display area and scratch on metal bezel, backlight module or polarizer film out of the display area, etc., are not counted. A <u>12-2-2 Bright spots</u> (1) Bright spots by the defect of TFT. · Visible under bias of 2% ND filter High bright spot R•G · Visible under 5% but invisible under 2% ND filter Low bright spot R•G•B · Invisible under bias of 5% ND filter Not counted (2) Bright spots by the light passing through tears, breaks, etc in color filter. · Exceed size of a half dot High bright spot · A half dot or less Not counted (3) Bright spots by the light passing through tears, breaks, etc in chromium mask. · Exceed 50μm High bright spot · 50μm or less Not counted B <u>12-2-3 Test condition</u> · Inspector must observe the LCD screen from the normal direction under the illumination by a single 20W fluorescent lamp. The distance between the LCD screen and the inspector should be a height of 50cm above the worktable. The vertical illuminance is 300 to 600lux (reference value). · Bright spot should be counted under entire black screen. · Dark spot should be counted under entire white screen. · Input signal timing should be typical value. C (Note1) Please do not mistake a single bright spot for a bright spot connection due to Cs(supplemental capacitance) line at the center of each dot. (Note2) If a pixel is dark partially, it connects into the number of dark spots in accordance with following rule. (a) $A < 1/3$ (b) $1/3 \leq A < 2/3$ (c) $2/3 \leq A$: Not count. Only one of 4 dark connection is allowed. : Considered as 0.5 dot. : Considered as 1 dot. (A=Dark spot size/dot size) D (Note1) Please do not mistake a single bright spot for a bright spot connection due to Cs(supplemental capacitance) line at the center of each dot. (Note2) If a pixel is dark partially, it connects into the number of dark spots in accordance with following rule. (a) $A < 1/3$ (b) $1/3 \leq A < 2/3$ (c) $2/3 \leq A$: Not count. Only one of 4 dark connection is allowed. : Considered as 0.5 dot. : Considered as 1 dot. (A=Dark spot size/dot size) E											
												F	
								TITLE FLC48SXC8V-10					
								DRAW. NO. Tech Bes LCD-00157				CUST.	
EDIT		DATE		DESIG.		CHECK		APPR.		DESCRIPTION			
DESIG.						CHECK				APPR.			
1													

13. ENVIRONMENTAL SPECIFICATIONS

Table 13-1 show the environmental specifications.

Table 13-1 Environmental specifications

Item	Condition		Remark
Temperature	Operation ②	0~55℃	Temperature on surface of LCD panel (display area.)
	Storage	-20~60℃	
Humidity	Operation	20~85%RH	Maximum wet-bulb temperature should not exceed 29℃. No condensation.
	Storage	5~85%RH	
Vibration	Non-operation	10~500Hz, 1octave/ 20minute, 19.6m/s²(2G), 1.5mm max, 1hour each X, Yand Z directions.	For single module without package.
Shock *1	Non-operation	294m/s² (30G), 6ms, 1time each ±X, ±Y and ±Z directions.	

NOTE：Table 13-2 and Figure 13-1 show the shock resistance standard when module is packaged.

Table 13-2 Shock resistance standard when module is packaged

Dropping location	Dropping height	Count
A~J	60cm	1 time

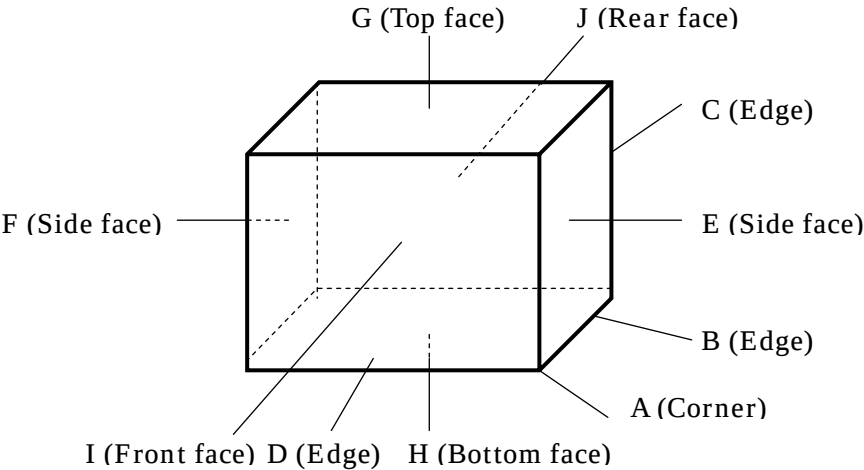


Figure 13-1 Direction to apply shock to package

DOCUMENT CONTROL SECTION

DATE

						TITLE FLC48SXC8V-10	
						DRAW. NO. Tech Bes LCD-00157	
						CUST.	
02	20021101				Change operation temperature.		
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION	FUJITSU DISPLAY TECHNOLOGIES CORPORATION	
DESIG.			CHECK		APPR.		22 /

14. INDICATIONS

This module has the following indications.

- (1) Product name : LCD unit
- (2) Model Number : FLC48SXC8V-10
- (3) Product Drawing Number : NA19026-C251
- (4) Manufacturing Number : 2Y00001

Serial number
(To be reset every month on 1st.)

Manufacturing month
(Oct. = X, Nov. =Y, Dec. =Z)

Last digit of manufacturing year.

- (5) Version number : 01A (Example)
-1st 2 digits "01" means operational version.
-3rd alphabet means functional version.
- (6) Manufacturer Country Name : MADE IN JAPAN
- (7) Company Name : FUJITSU DISPLAY TECHNOLOGIES CORP.
- (8) Disposal method of cold-cathode tubes.
- (9) Caution when changing cold-cathode tubes.

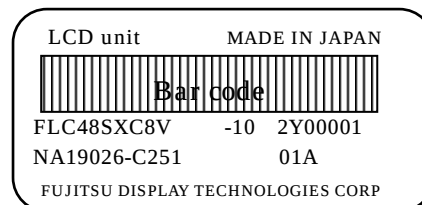


Figure 14-1 Product Label (Example)

15. PACKAGING

15-1 Packing specifications

- (1) 5 LCD modules/1package.
- ②(2) Weight:approximately 13kg/1package.
- (3) Outline dimensions: 534mm (W)x329mm (D)x 480mm (H)

15-2 Packing method

Figure 15-2 show the packing method.

DOCUMENT CONTROL SECTION

DATE

						TITLE FLC48SXC8V-10					
						DRAW. NO. Tech Bes LCD-00157				CUST.	
02	20021101				Change package weight.						
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION					FUJITSU DISPLAY TECHNOLOGIES CORPORATION	SHEET 23 /
	DESIG.			CHECK			APPR.				

1

2

3

4

A

A

Protective sheet

Front side

B

B

Put the cable in slot

Rear side

C

C

D

D

Anti-Electric Bag

Front side

E

Fig.15-2 (a) Packaging Method

DOCUMENT CONTROL SECTION

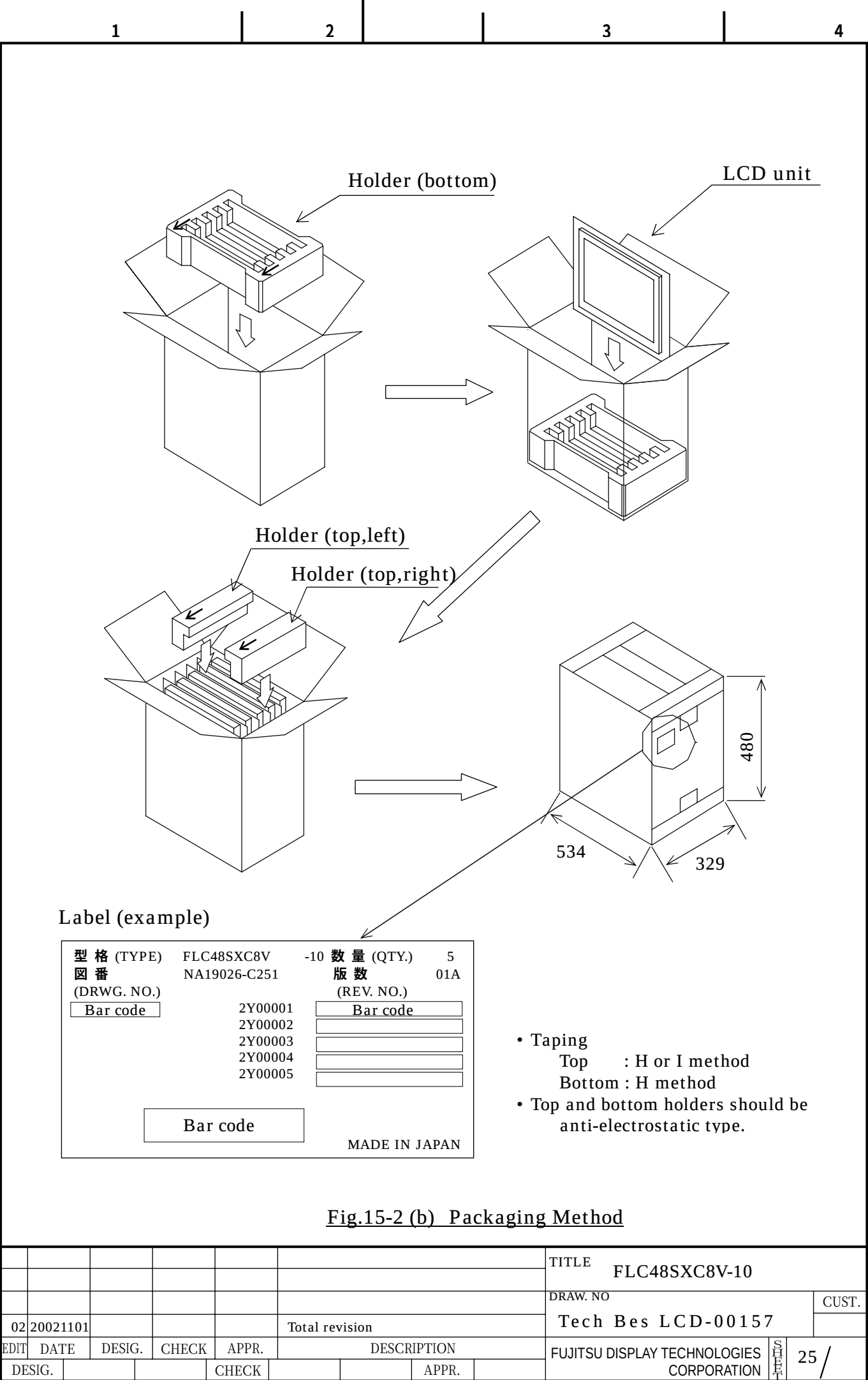
DATE

02	20021101				Total revision
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION
DESIG.			CHECK		APPR.

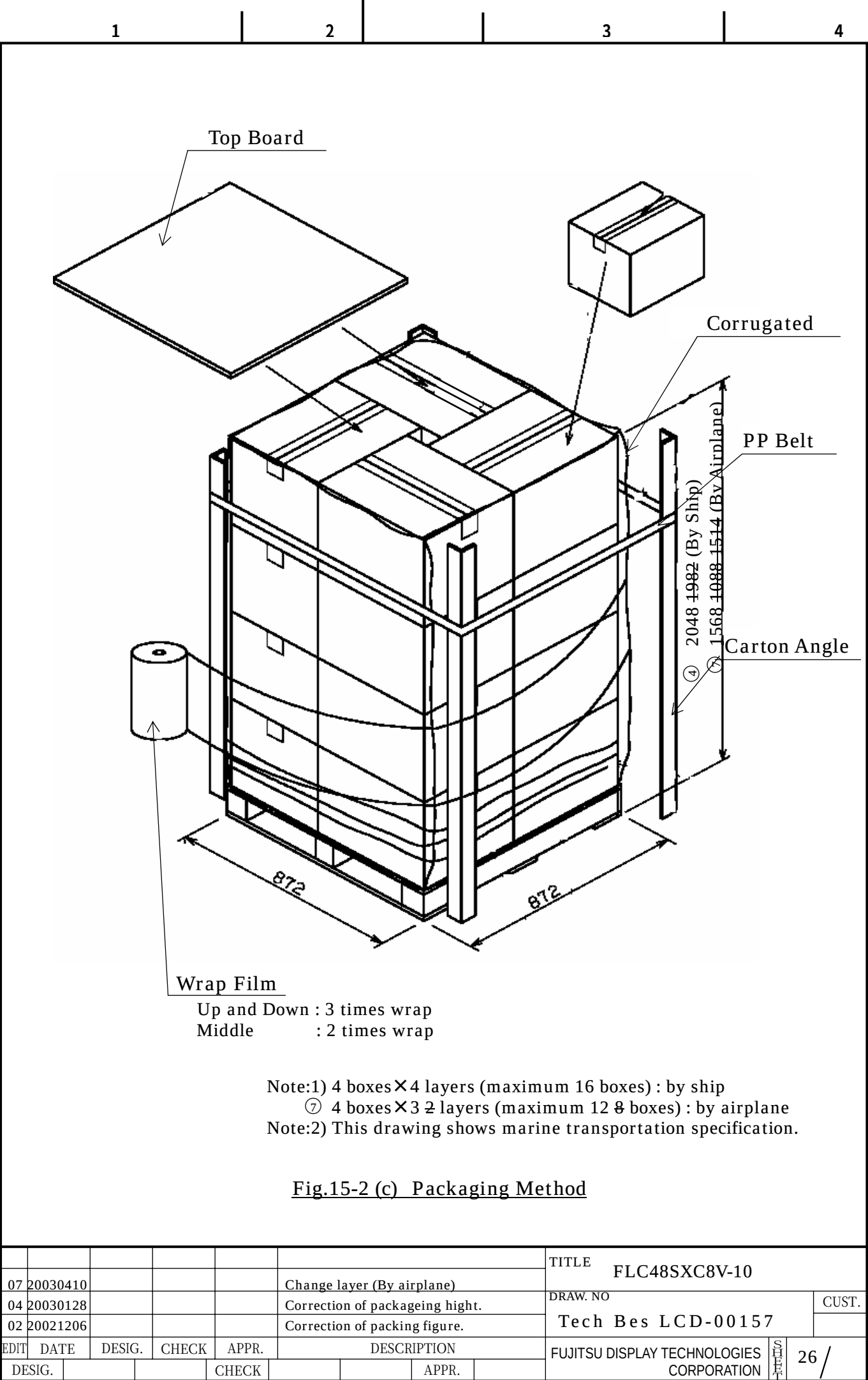
TITLE		FLC48SXC8V-10		
DRAW. NO		Tech Bes LCD-00157		CUST.
FUJITSU DISPLAY TECHNOLOGIES CORPORATION		24 /		

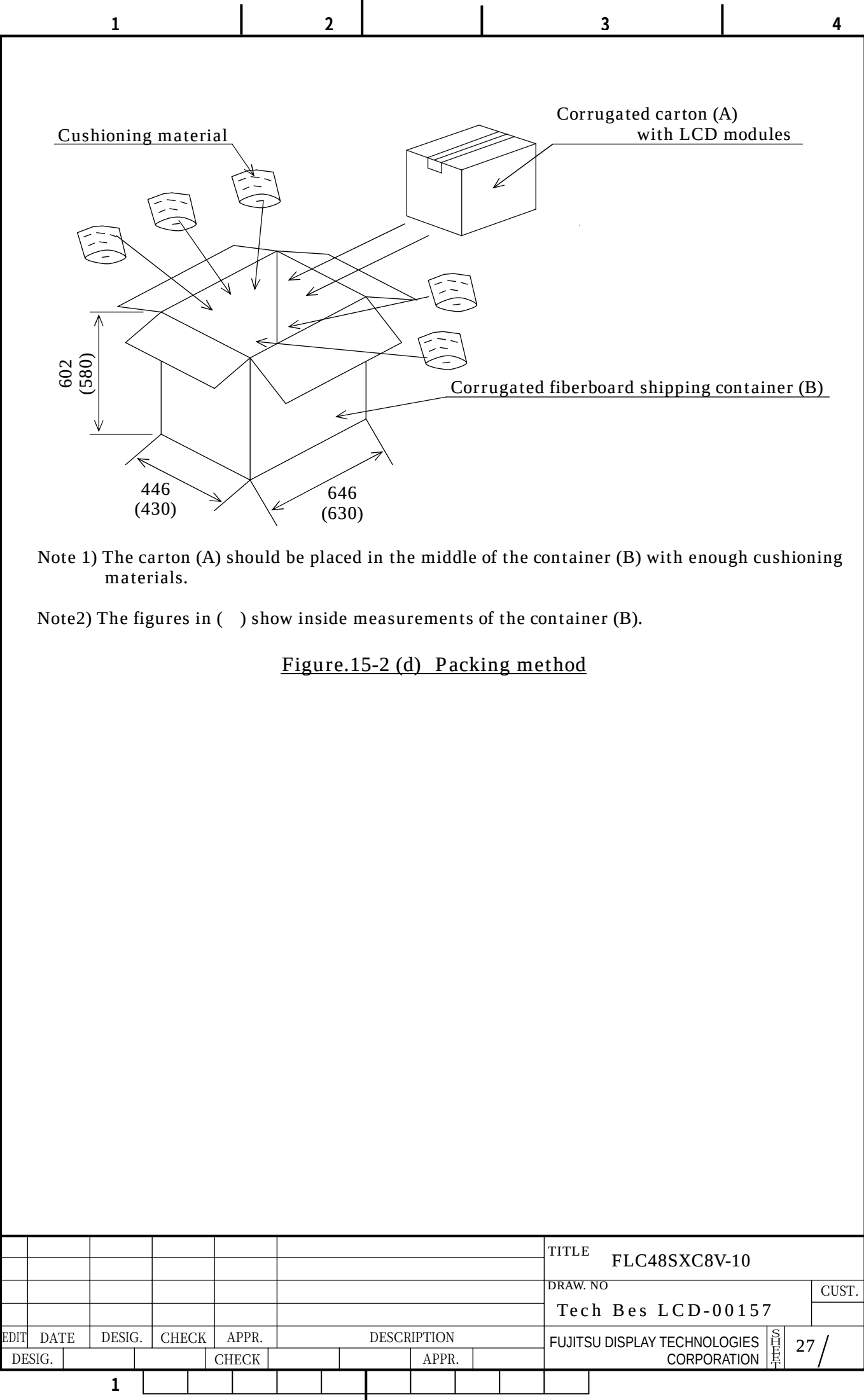
F

1



DATE	DOCUMENT CONTROL SECTION				





A

A

B

B

C

c

D

- D

E

- F**

Do not use unspecified solvent such as ketone (acetone, etc.) and aromatics (xylene, toluene, etc.)

DATE	DOCUMENT CONTROL SECTION

						TITLE FLC48SXC8V-10						
						DRAW. NO Tech Bes LCD-00157						CUST.
08	20030513				Add the pressure spec.							
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION					FUJITSU DISPLAY TECHNOLOGIES CORPORATION		28 /
	DESIG.			CHECK			APPR.					

A

- B**

B

C

C

- D**

1

D

- E

F

- 1

DOCUMENT CONTROL SECTION

DATE _____

						TITLE FLC48SXC8V-10									
						DRAW. NO							CUST.		
						Tech Bes LCD-00157									
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION							FUJITSU DISPLAY TECHNOLOGIES CORPORATION	Sheet	30 /	
	DESIG.			CHECK			APPR.								

A

- In a corrosive gas environment, various parts of the module may corrode or deteriorate.

- The LCD module is in an anti-static bag. Keep the module in that status.

- B**

B

- Note) If the module is left in an environment of 60°C and above for a long period of time, optical characteristics may deteriorate.

C

- C

The components of this LCD module can be grouped into metal, resin, glass and so on. As the backlight contains CCFL which includes mercury, it must be disposed according to the local ordinance or regulations.

- D**

D

E

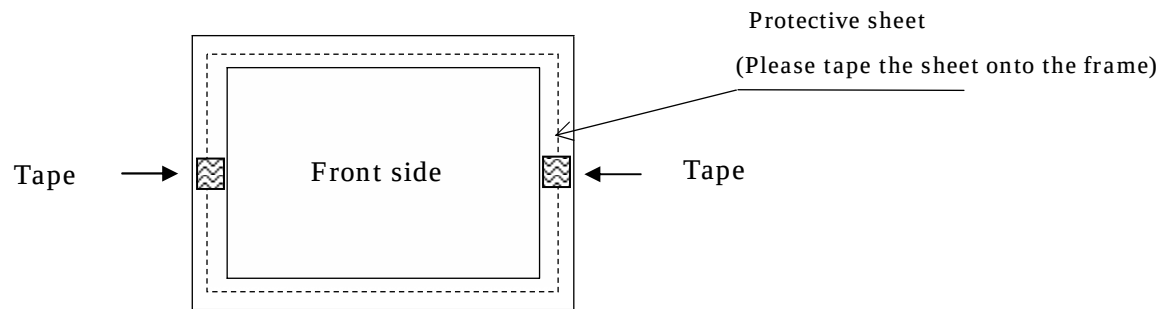
F

1 2 3 4

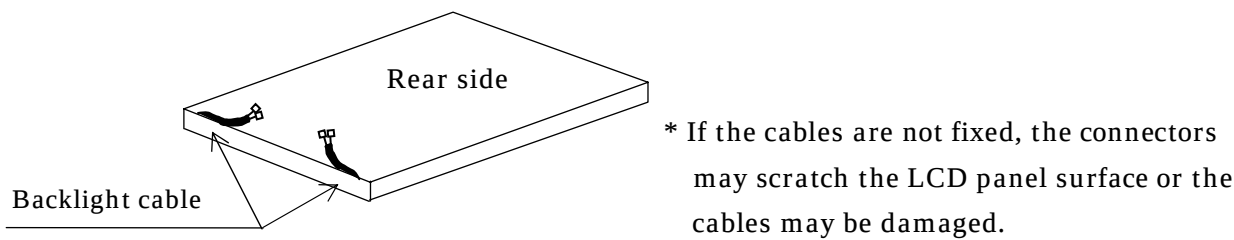
(8) Return method of the LCD module requested for repair or analysis of the problem

- A
- When returning the LCD modules, adhere to the following procedures not to damage the LCD panel or the backlight cables. (Fig. 17-1(a)~(b))
- When the LCD module is returned without following the specified packaging procedures, FDTC will not take responsibility for the damages caused by the failure of the packaging method.

(1) Attach protective sheet.



(2) Put the backlight cables in slots.



(3) Put the LCD module into the anti-electrostatic bag
(Please do not use torn anti-electrostatic bags)

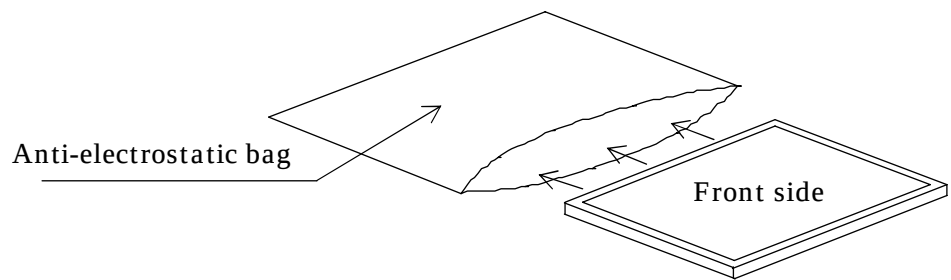


Fig. 17-1(a) Packaging method

DOCUMENT CONTROL SECTION

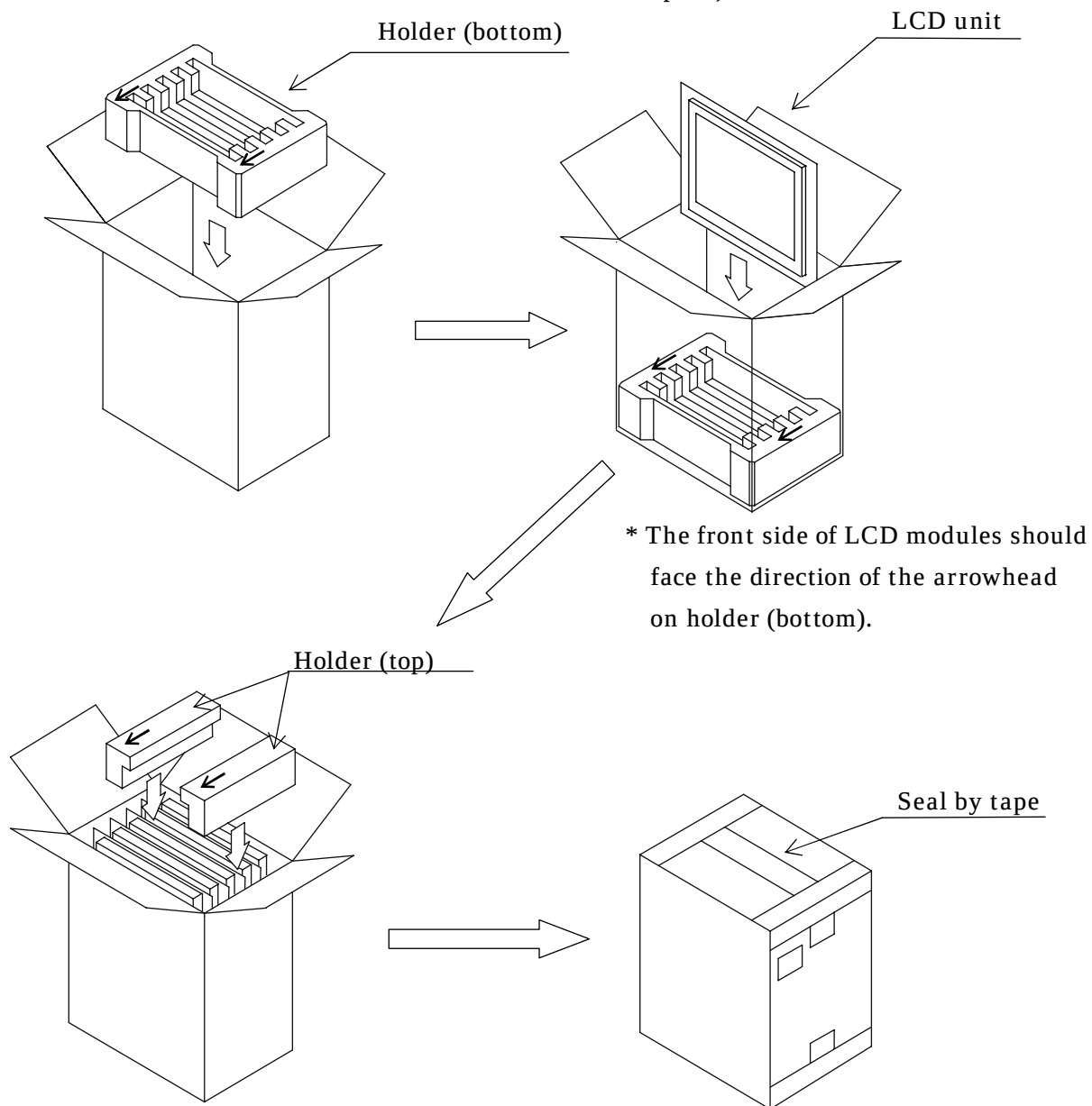
DATE

						TITLE		FLC48SXC8V-10	
						DRAW. NO		CUST.	
						Tech Bes LCD-00157			
02	20021101					Total revision			
EDIT	DATE	DESIG.	CHECK	APPR.		DESCRIPTION		FUJITSU DISPLAY TECHNOLOGIES CORPORATION	
DESIG.				CHECK			APPR.		32 /

(4) Storage into the carton box

- When using the carton box manufactured by FDTC

(Please use carton boxes and arrowheads that are not collapsed)



- * The direction of the arrowhead on holder (top) should face the front side of the LCD modules.

****The arrowheads are shown on the holders.****

Fig. 17-1(b) Packaging method

- When not using the carton box manufactured by FDTC

Please pack the LCD modules one by one and make sure not to damage the LCD modules when transporting.

DOCUMENT CONTROL SECTION

DATE

						TITLE		FLC48SXC8V-10	
						DRAW. NO		Tech Bes LCD-00157	
						CUST.			
02	20021101					Total revision			
EDIT	DATE	DESIG.	CHECK	APPR.		DESCRIPTION			
DESIG.				CHECK		FUJITSU DISPLAY TECHNOLOGIES CORPORATION		33 /	

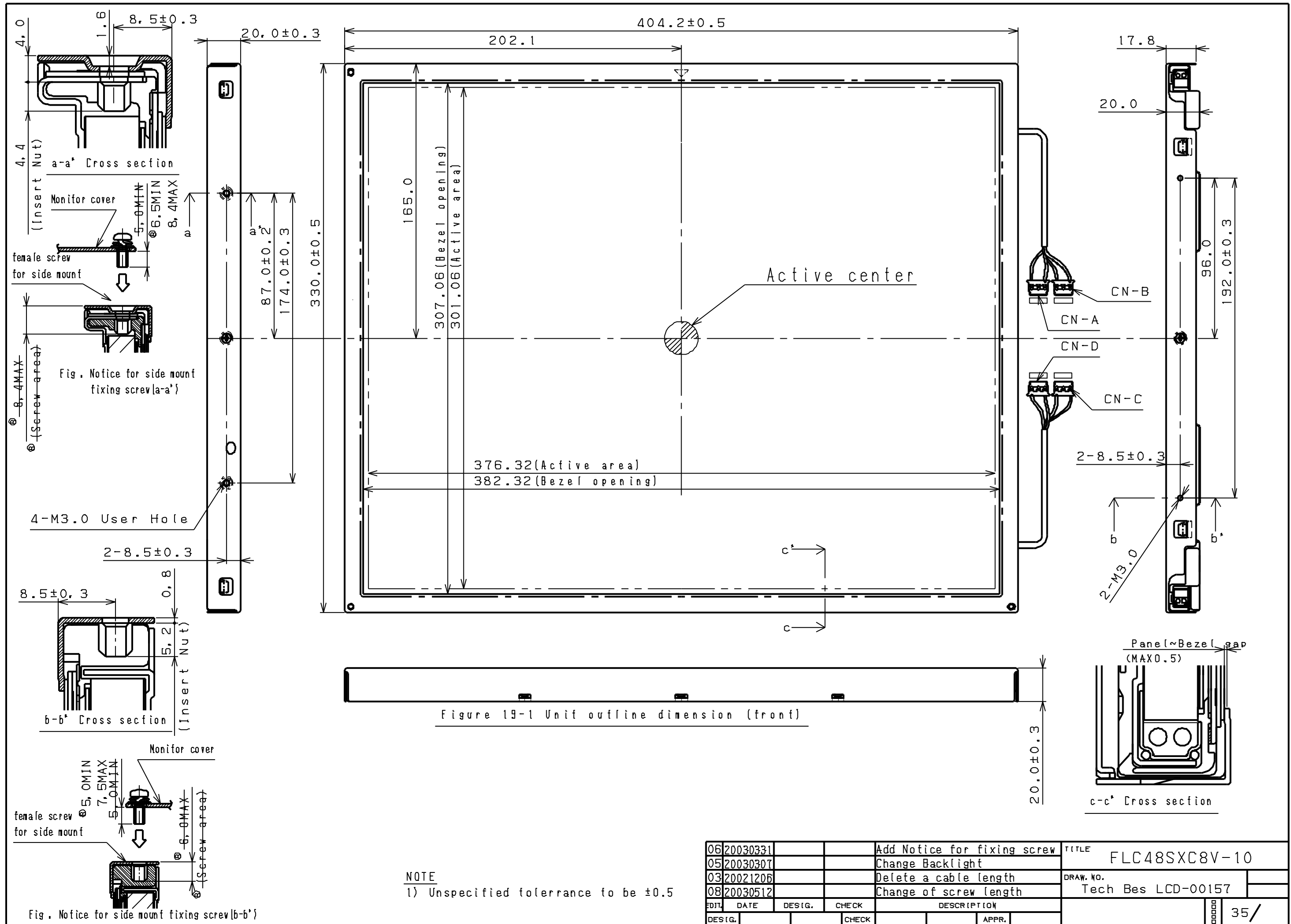
② Flux residue on the printed circuit board is harmless to the quality and reliability of LCD module.
Fujitsu has adopted non-wash technology on module assembly process.

This Product is designed, developed and manufactured as contemplated for general use, including without limitation, general office use, personal use, household use, and ordinary industrial use, but is not designed, developed and manufactured as contemplated for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (hereinafter “High Safety Required Use”), including without limitation, nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system. If customer’s product possibly falls under the category of High Safety Required Use, please consult with our sales representatives in charge before such use. In addition, Fujitsu shall not be liable against the Customer and/or any third party for any claims or damages arising in connection with the High Safety Required Use of the Product without permission.

Specifications of the TFT-LCD panel and other components used in the LCD module are subject to change. Both parties shall discuss together before change.

If any doubt is raised in the content of the specifications, both parties shall discuss and make best effort for the agreement.

[illegible]



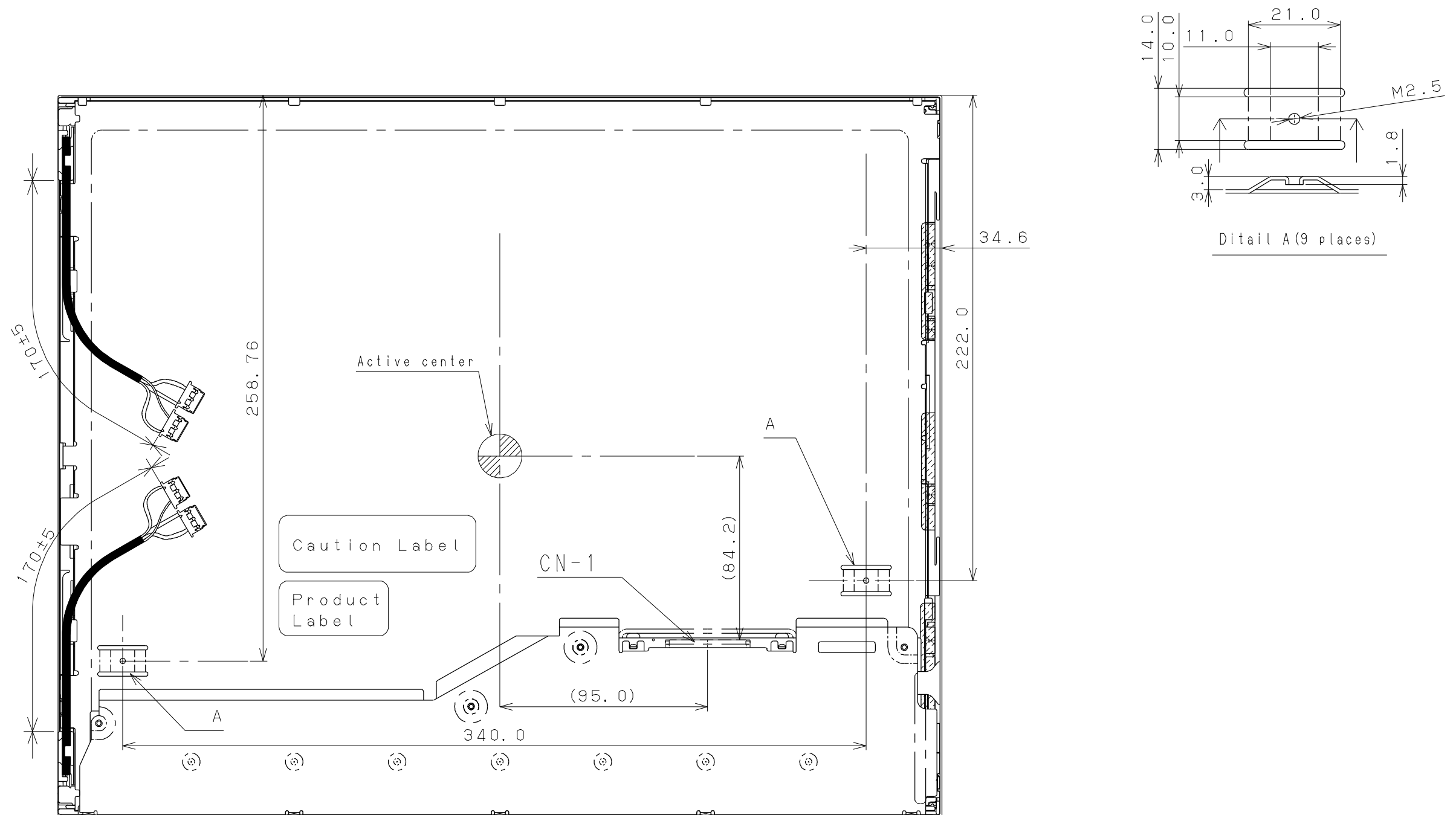


Figure 19-2 Unit outline dimension (back)

					TITLE				FLC48SXC8V-10	
05	20030307			Change Backlight				DRAW. NO.		
03	20021206			Total Revision						
02	20021101			Total Revision				Tech Bes LCD-00157		
EDIT.	DATE	DESIG.	CHECK	DESCRIPTION						36 / 36
DESIG.			CHECK			APPR.				