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SPECIFICATION
FOR
APPROVAL

(●) **Preliminary Specification**
( ) **Final Specification**

Title	17.3” Full HD TFT LCD

BUYER	HP
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP173WF2
Suffix	TPB1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
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Product Engineering Dept.
LG Display Co., Ltd

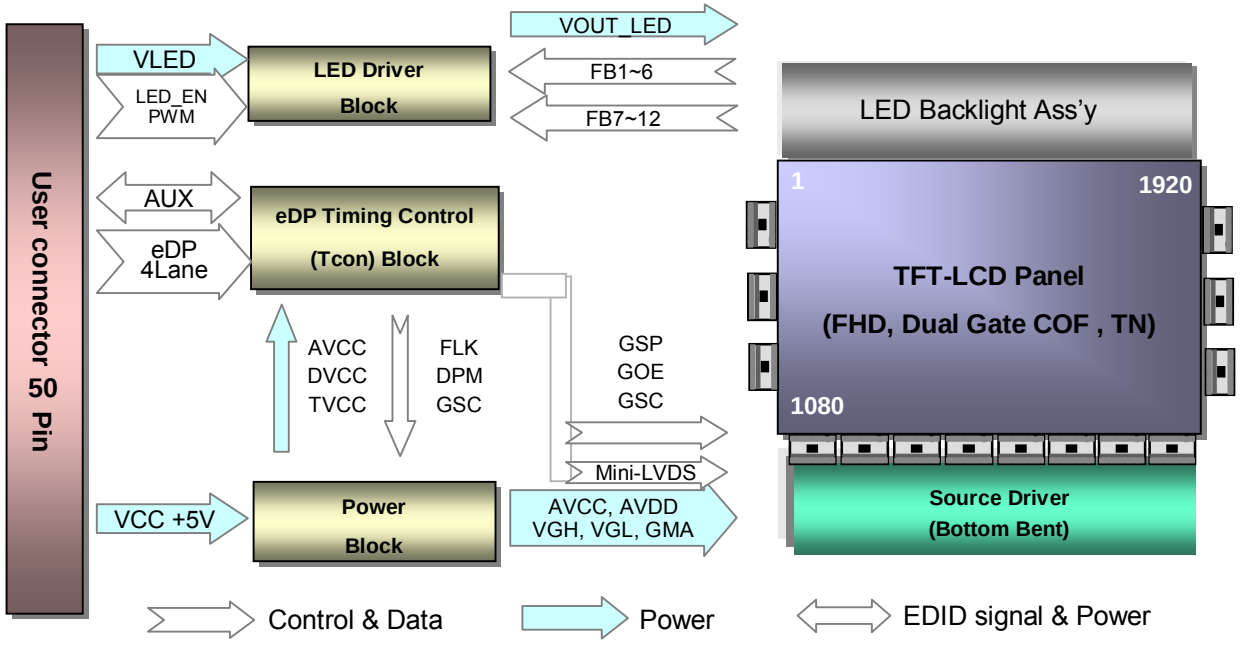
Contents

RECORD OF REVISIONS

Revision No	Revision Date	Page	Description	EDID ver
0.0	Feb. 11. 2010	-	First Draft (Preliminary Specification)	-
0.1	May.05.2010	8	Change connector pinmap	
		10	Update TIMING TABLE	
		31-33	Update EEDID data	V0.1

1. General Description

The LP173WF2 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 17.3 inches diagonally measured active display area with FHD resolution (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP173WF2 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP173WF2 is intended to support applications where thin thickness, high brightness are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP173WF2 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	17.3 inches diagonal
Outline Dimension	381.888(Typ. H) × 214.812(Typ. V) × 6.5(D, Max.) [mm]
Pixel Pitch	0.199 × 0.199 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	400 cd/m^2(Typ.)
Power Consumption	Total 2D TBD W/ 3D TBD W(Typ.)
Weight	650g(Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Anti-Glare treatment of the front Polarizer
RoHS Compliance	Yes
BFR / PVC / As Free	Yes for all.

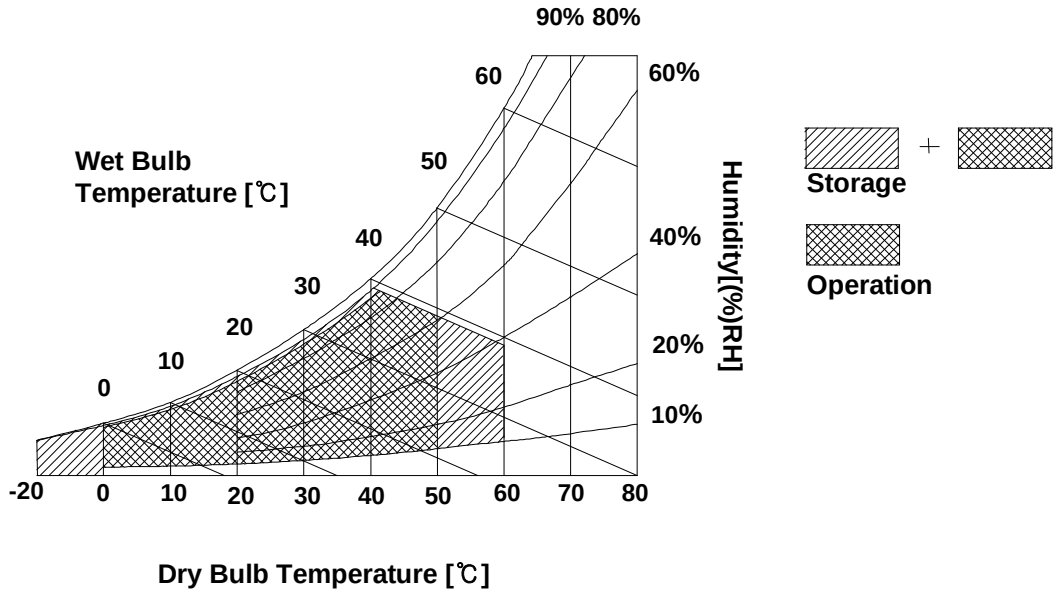
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

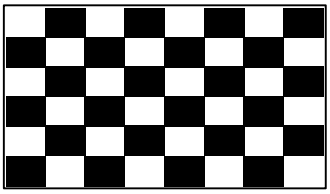
The LP173WF2 requires two power inputs. The first logic is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second backlight is the input about LED BL with LED Driver.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LOGIC :							
Power Supply Input Voltage		V_{CC}	4.5	5.0	5.5	V	1
Power Supply Input Current (2D) : Not Fixed	Mosaic	I_{CC} _60Hz	-	TBD	920	mA	2
	Black		-	TBD	1260		
Power Supply Input Current (3D) : Not Fixed	Mosaic	I_{CC} _120Hz + VBI	-	TBD	1620		
	Black		-	TBD	2300		
Power Consumption (2D) : Not Fixed	Mosaic	P_{CC} _60Hz	-	TBD	4.6	W	
	Black		-	TBD	6.3		
Power Consumption(3D) : Not Fixed	Mosaic	P_{CC} _120Hz+VBI	-	TBD	8.1		
	Black		-	TBD	11.5		
Power Supply Inrush Current		I_{CC_P}	-	-	TBD	mA	3
eDP Impedance		Z_{eDP}	90	100	110	Ω	4
BACKLIGHT : (with LED Driver)							
LED Power Input Voltage		V_{LED}	7.0	12.0	21.0	V	5
LED Power Input Current : Not Fixed		I_{LED}	-	TBD	970	mA	6
LED Power Consumption : Not Fixed		P_{LED}	-	TBD	11.6	W	6
LED Power Inrush Current		I_{LED_P}	-	-	1000	mA	7
PWM Duty Ratio			5	-	100	%	8
PWM Jitter		-	0	-	0.2	%	9
PWM Impedance		Z_{PWM}	20	40	60	kΩ	
PWM Frequency		F_{PWM}	TBD	-	1000	Hz	10
PWM High Level Voltage		V_{PWM_H}	3.0	-	3.6	V	
PWM Low Level Voltage		V_{PWM_L}	0	-	0.3	V	
LED_EN Impedance		Z_{PWM}	20	40	60	kΩ	
LED_EN High Voltage		$V_{LED\_EN\_H}$	3.0	-	3.6	V	
LED_EN Low Voltage		$V_{LED\_EN\_L}$	0	-	0.3	V	
Life Time			12,000	-	-	Hrs	11

Note)

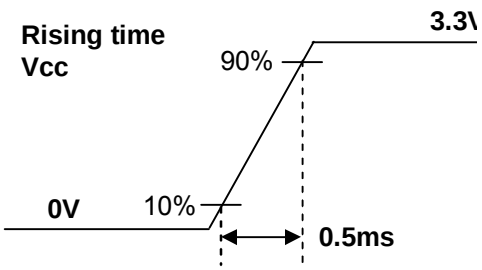
1. The measuring position is the connector of LCM and the test conditions are under 25℃, fv = 60Hz.
2. The specified Icc current and power consumption are under the Vcc = 5V , 25℃, fv = 60Hz or 120Hz+VBI condition.

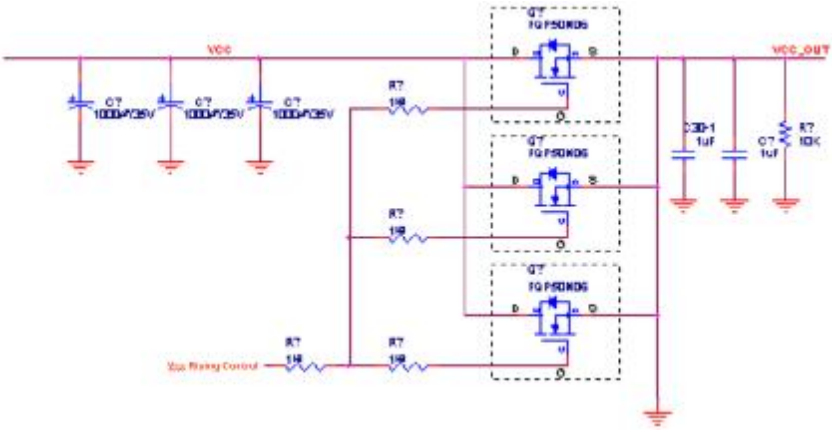


White Pattern

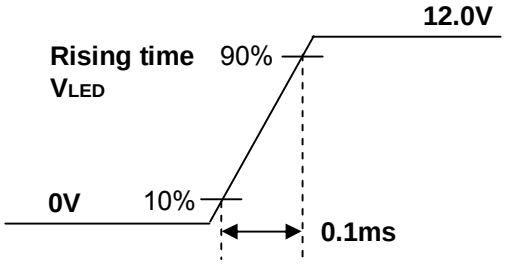
Black Pattern

3. This Spec. is the max load condition for the cable impedance designing.
4. The below figures are the measuring Vcc condition and the Vcc control block LGD used.
   The Vcc condition is same as the minimum of T1 at Power on sequence.





5. This impedance value is needed for proper display and measured form eDP Tx to the mating connector.
6. The measuring position is the connector of LCM and the test conditions are under 25℃.
7. The current and power consumption with LED Driver are under the Vled = 12.0V , 25℃, Dimming of Max luminance and White pattern with the normal frame frequency operated(60Hz).
8. The below figures are the measuring Vled condition and the Vled control block LGD used.
   VLED control block is same with Vcc control block.

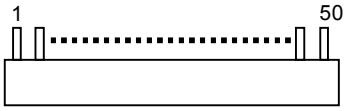


9. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
10. If Jitter of PWM is bigger than maximum, it may induce flickering.
11. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
12. The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 7. under general user condition.

3-2. Interface Connections

This LCD employs two interface connections, a 50 pin connector used for the module electronics interface and the other connector used for the integral backlight system.

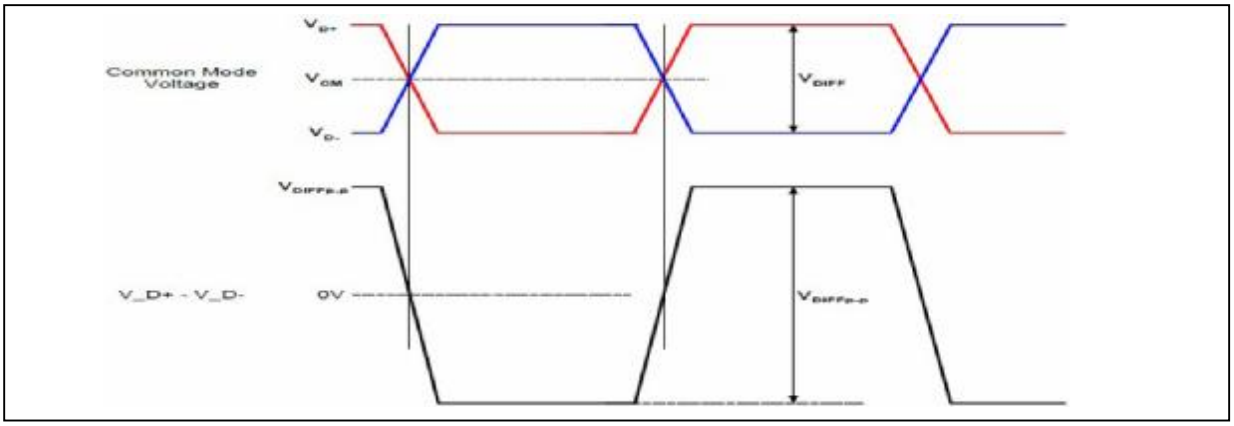
Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	2D_3D	2D/3D Contents communica ion	**[Interface Chip]** 1. LCD : MStar, MST7329Y(LCD Controller) Including eDP Receiver. 2. System : TBD or equivalent **[Connector]** JAE FI-VHP50 or equivalent **[Mating Connector]** JAE FI-VHP50 series or equivalent (micro-coax type) **[Connector pin arrangement]**  [LCD Module Rear View]
2	GND	Ground	
3	VLED	LED Power Supply 7V ~ 20V	
4	VLED	LED Power Supply 7V ~ 20V	
5	VLED	LED Power Supply 7V ~ 20V	
6	VLED	LED Power Supply 7V ~ 20V	
7	GND	Ground	
8	Data I2C	Data I2C (Pvcom, Pgamma Setting)	
9	CLK I2C	CLK I2C (Pvcom, Pgamma Setting)	
10	PWM	PWM for Luminance Control	
11	LED_EN	Back Light On/Off Control	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	GND	Ground	
16	HPD	Hot Plug Detection pin	
17	GND	Ground	
18	NC	No Connection (Reserved)	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	VCC	Power Supply (5.0V typ.)	
24	VCC	Power Supply (5.0V typ.)	
25	VCC	Power Supply (5.0V typ.)	
26	VCC	Power Supply (5.0V typ.)	
27	VCC	Power Supply (5.0V typ.)	
28	VCC	Power Supply (5.0V typ.)	
29	VCC	Power Supply (5.0V typ.)	
30	VCC	Power Supply (5.0V typ.)	
31	VCC	Power Supply (5.0V typ.)	
32	VCC	Power Supply (5.0V typ.)	
33	GND	Ground	
34	AUX_CH_N	Complement Signal-Auxiliary Channel	
35	AUX_CH_P	True Signal-Auxiliary Channel	
36	GND	Ground	
37	Lane0_P	True Signal-Main Lane 0	
38	Lane0_N	Complement Signal-Lane 0	
39	GND	Ground	
40	Lane1_P	True Signal-Main Lane 1	
41	Lane1_N	Complement Signal-Lane 1	
42	GND	Ground	
43	Lane2_P	True Signal-Main Lane 2	
44	Lane2_N	Complement Signal-Lane 2	
45	GND	Ground	
46	Lane3_P	True Signal-Main Lane 3	
47	Lane3_N	Complement Signal-Lane 3	
48	GND	Ground	
49	NC	No connect.	
50	NC	No connect.	

3-3. eDP Signal Timing Specifications

3-3-1. DC Specification

The VESA Display Port related AC specification is compliant with the VESA Display Port Standard v1.1a.



Description	Symbol	Min	Max	Unit	Notes
Differential peak-to-peak Input voltage	VDIFF p-p	120	-	mV	For high bit rate
		40	-		For reduced bit rate
Rx DC common mode voltage	VCM	0	2.0	V	-

3-3-2. AC Specification

The VESA Display Port related AC specification is compliant with the VESA Display Port Standard v1.1a.

Description	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate (2.7Gbps/lane)	UI_High_Rate	-	370	-	ps	Range is nominal ±350ppm. DisplayPort Link Rx does not require local crystal for link clock generation
Unit Interval for high bit rate (1.62Gbps/lane)	UI_Low_Rate	-	617	-	ps	
Lane-to-Lane skew	V Rx-SKEW-INTER_PAIR	-	-	5200	ps	-
Lane intra-pair skew	V Rx-SKEW-INTRA_PAIR	-	-	100	ps	For high bit rate
		-	-	300	ps	For reduced bit rate

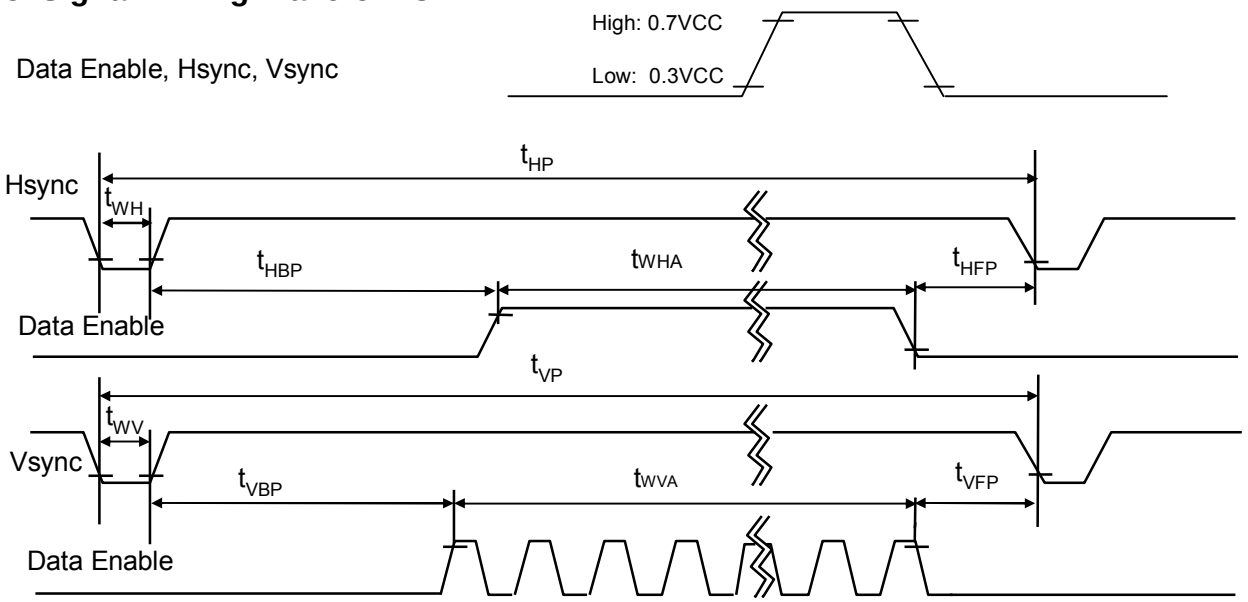
3-4. Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 4. TIMING TABLE

ITEM	Symbol		Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	f_{CLK}	-	37.1	100	MHz	2D (145MHz@60Hz) 3D (396MHz@120+VBI)
Hsync	Period	t_{HP}	TBD	550	TBD	tCLK	Not Fixed
	Width	t_{WH}	TBD	11	TBD		
	Width-Active	tw_{HA}	480	480	480		
Vsync	Period	t_{VP}	TBD	1125	TBD	tHP	Not Fixed
	Width	t_{WV}	TBD	5	TBD		
	Width-Active	tw_{VA}	1080	1080	1080		
Data Enable	Horizontal back porch	t_{HBP}	TBD	37	TBD	tCLK	Not Fixed
	Horizontal front porch	t_{HFP}	TBD	22	TBD		Not Fixed
	Vertical back porch	t_{VBP}	TBD	36	TBD	tHP	Not Fixed
	Vertical front porch	t_{VFP}	TBD	4	TBD		Not Fixed

3-5. Signal Timing Waveforms



3-6. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	…			…						…						…			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...			…						…						…			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…			…						…						…			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-7. Power Sequence

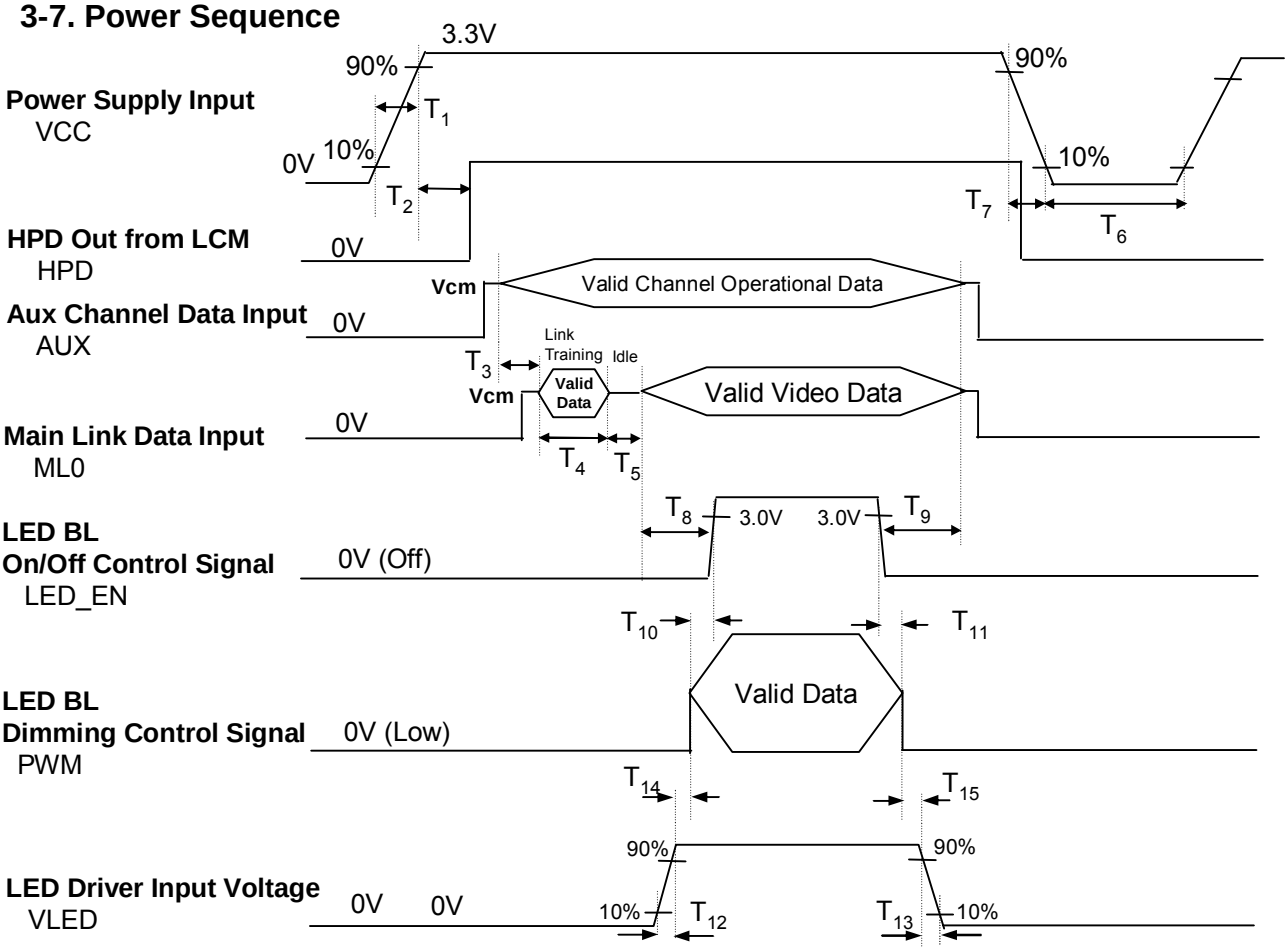


Table 6. POWER SEQUENCE TABLE

Logic Parameter	Value			Units	LED Parameter	Value			Units
	Min.	Typ.	Max.			Min.	Typ.	Max.	
T_1	0.5	-	10	ms	T_9	200	-	-	ms
T_2	0	-	200	ms	T_{10}	0	-	-	ms
T_3	50	75	-	ms	T_{11}	0	-	-	ms
T_4	0	-	-	ms	T_{12}	0.5	-	-	ms
T_5	0	-	-	ms	T_{13}	0	-	5000	ms
T_6	500	-	-	ms	T_{14}	10	-	-	ms
T_7	3	-	10	ms	T_{15}	10	-	-	ms
T_8	200	-	-	ms					

Note)
1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. eDP Signal Timing Specifications"
3. LVDS, LED_EN and PWM need to be on pull-down condition on invalid status.
4. LGD recommend the rising sequence of VLED after the Vcc and valid status of LVDS turn on.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

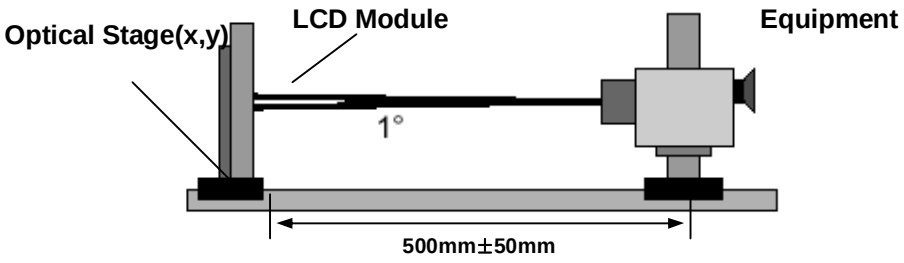


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 69.3MHz

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	500	-	-		1
Surface Luminance, white		L_{WH}	340	400	-	cd/m^2	2
Luminance Variation		δ_{WHITE}	-	1.4	1.6	%	3
Response Time	Black to White	$Tr_R + Tr_D$	-	5	12	ms	4
	Gray to Gray	$Tr_R + Tr_D$	-	TBD	6	ms	5
Color Coordinates							
	RED	RX	TBD	TBD	TBD		
		RY	TBD	TBD	TBD		
	GREEN	GX	TBD	TBD	TBD		
		GY	TBD	TBD	TBD		
	BLUE	BX	TBD	TBD	TBD		
		BY	TBD	TBD	TBD		
	WHITE	WX	0.283	0.313	0.343		
		WY	0.299	0.329	0.359		
Viewing Angle							6
	x axis, right(Φ=0°)	Θr	60	-	-	degree	
	x axis, left (Φ=180°)	Θl	60	-	-	degree	
	y axis, up (Φ=90°)	Θu	50	-	-	degree	
	y axis, down (Φ=270°)	Θd	50	-	-	degree	
Gray Scale							7
Color Gamut		C/G	-	72	-	%	

Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$LWH = \text{Average}(L1, L2, \ldots L5)$$

3. The variation in surface luminance , The panel total variation (δ WHITE) is determined by measuring LN at each test position 1 through 13 and then defined as following numerical formula. For more information see FIG 2.

$$\delta \text{WHITE}(= \frac{\text{Maximum}(L1, L2, \ldots L13) - \text{Minimum}(L1, L2, \ldots L13)}{\text{Maximum}(L1, L2, \ldots L13)} * 100(\%)$$

4. Response time is the time required for the display to transition from white to black (rise time, TrR) and from black to white(Decay Time, TrD). For additional information see FIG 3.

5. The gray to gray response time is defined as the following table and shall be measured by switching the input signal for “Gray To Gray”.

- Gray step : 5 step
- TGTG (Typ) is the typical specification of total average time at rising time and falling time for ‘Gray to Gray’.
- TGTG (Max) is the maximum specification of total average time at rising time and falling time for ‘Gray to Gray’.

Gray to Gray		Rising Time				
		G63	G47	G31	G15	G0
Falling Time	G63					
	G47					
	G31					
	G15					
	G0					

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

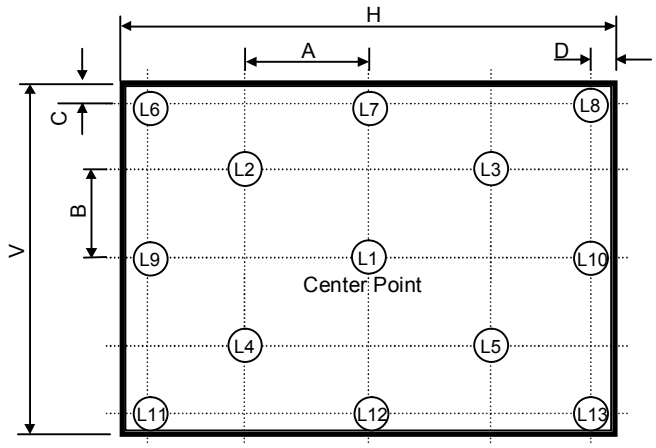
7. Gray scale specification

* fV = 60Hz

Gray Level	Luminance [%] (Typ)
L0	TBD
L7	TBD
L15	TBD
L23	TBD
L31	TBD
L39	TBD
L47	TBD
L55	TBD
L63	100

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
C : 10 mm
D : 10 mm
POINTS : 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

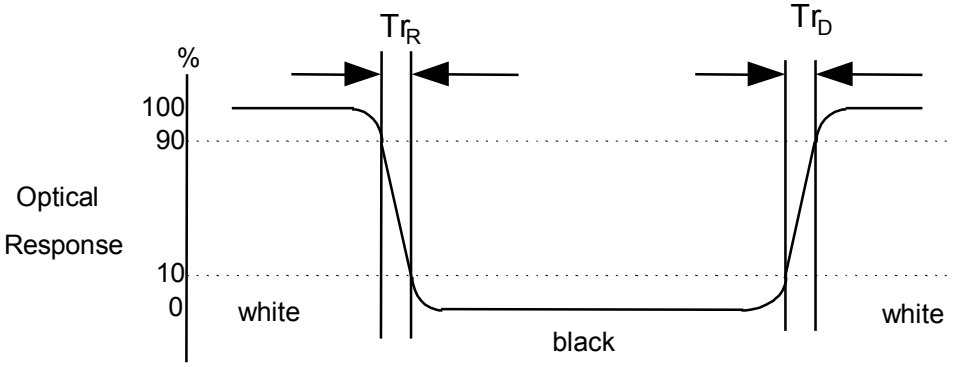
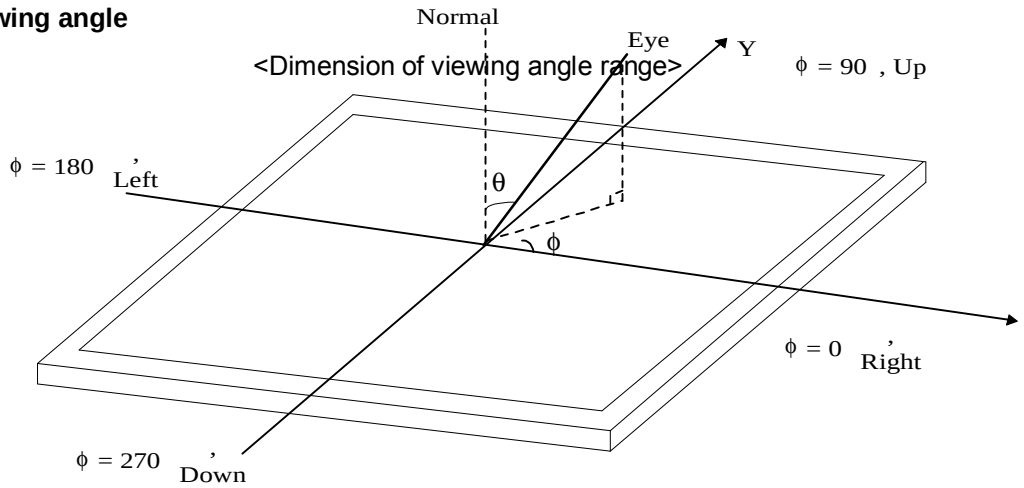


FIG. 4 Viewing angle



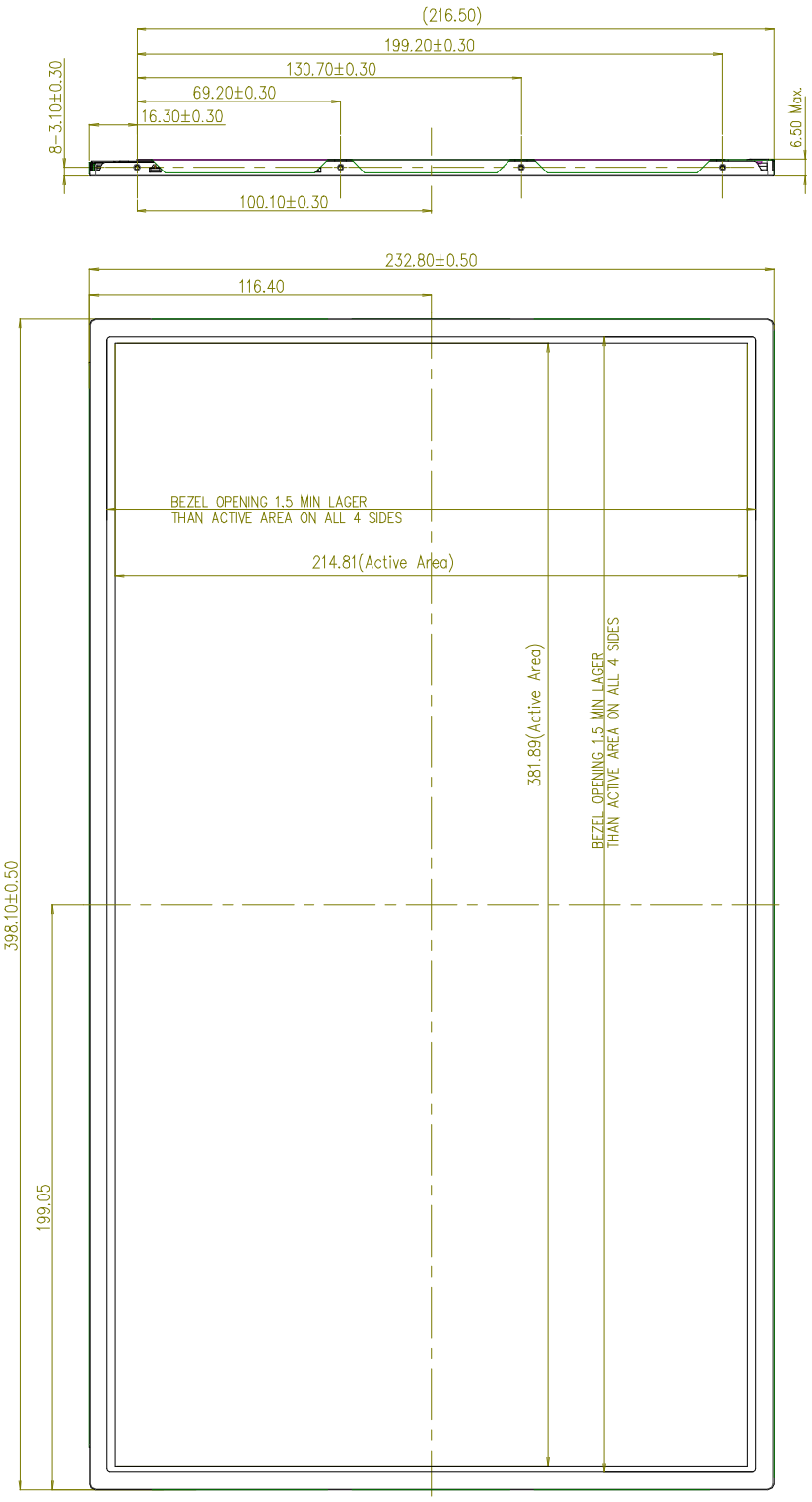
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP173WF2.
In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal (A)	398.1 ± 0.50mm
	Vertical (B)	232.8 ± 0.50mm
	Thickness	6.5mm(Max.)
Bezel Area	Horizontal	1.5mm Min.(Lager than Active Display Area)
	Vertical	1.5mm Min.(Lager than Active Display Area)
Active Display Area	Horizontal	381.89mm
	Vertical	214.81mm
Weight	650g (Max.)	
Surface Treatment	Anti-Glare treatment of the front polarizer (Haze 44%)	

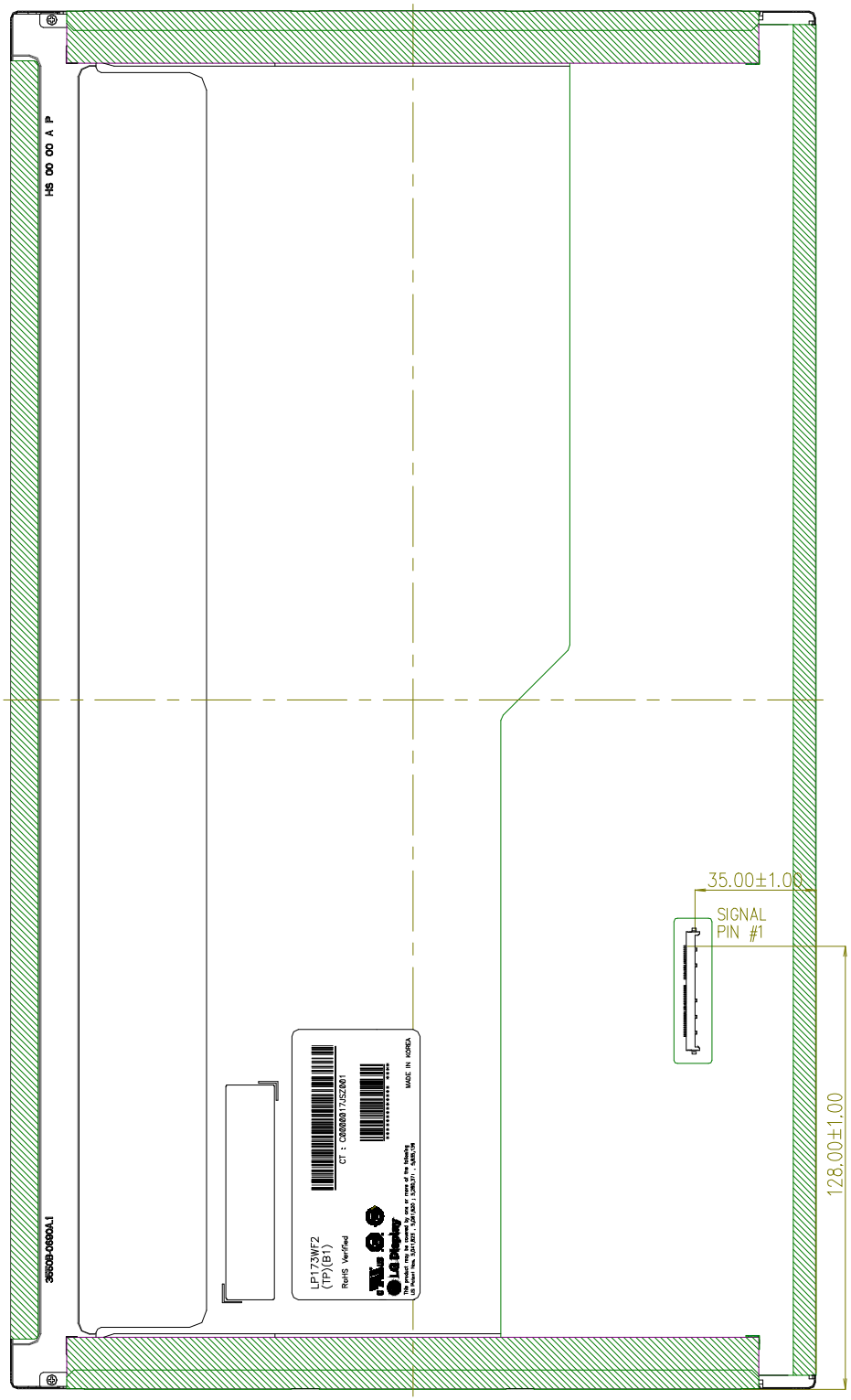
<FRONT VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm

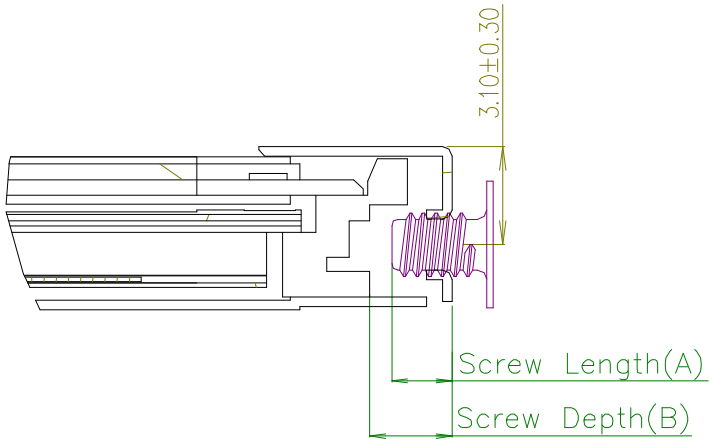


<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm



[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]

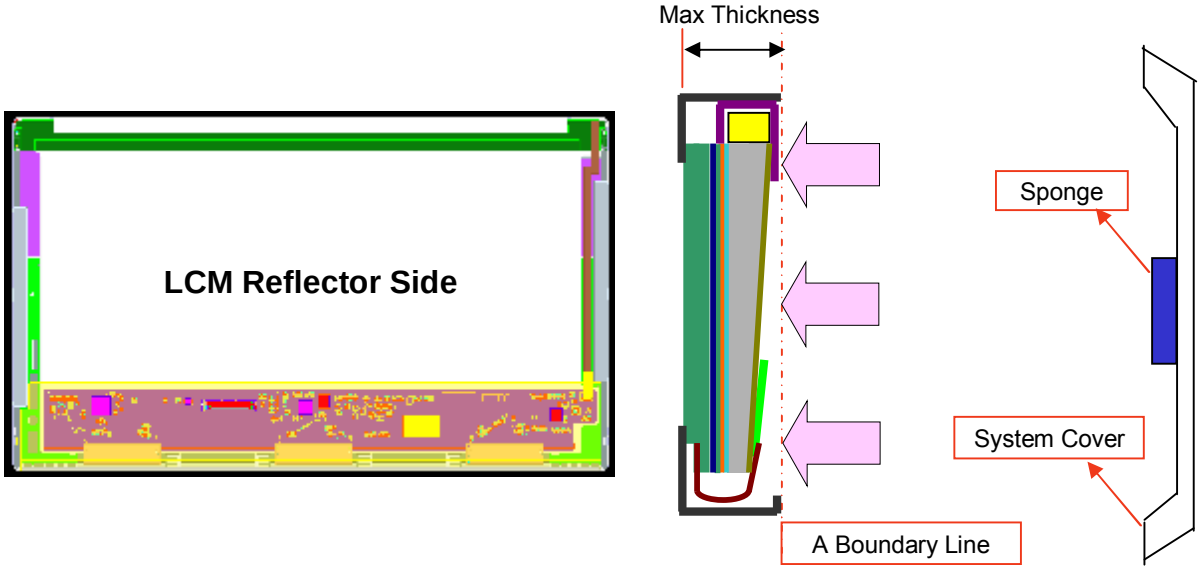


* Screw Length(A) : Max : 2.5, Min : 2.0
* Screw Depth(B) : Min 2.5
* Screw Torque : Max 2.5kgf.cm
(Measurement Gauge:Torque Meter)

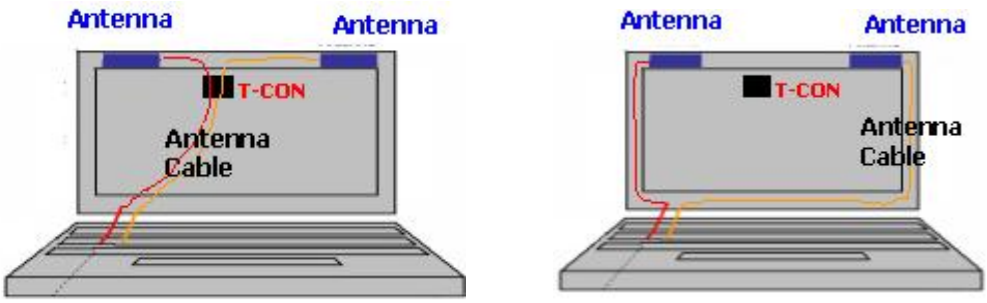
Notes : 1. Screw plated through the method of non-electrolytic nickel plating is preferred to reduce possibility that results in vertical and/or horizontal line defect due to the conductive particles from screw surface.

LGD Proposal for system cover design.(Appendix)

1	Gap check for securing the enough gap between LCM and System cover.	



Notes	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.

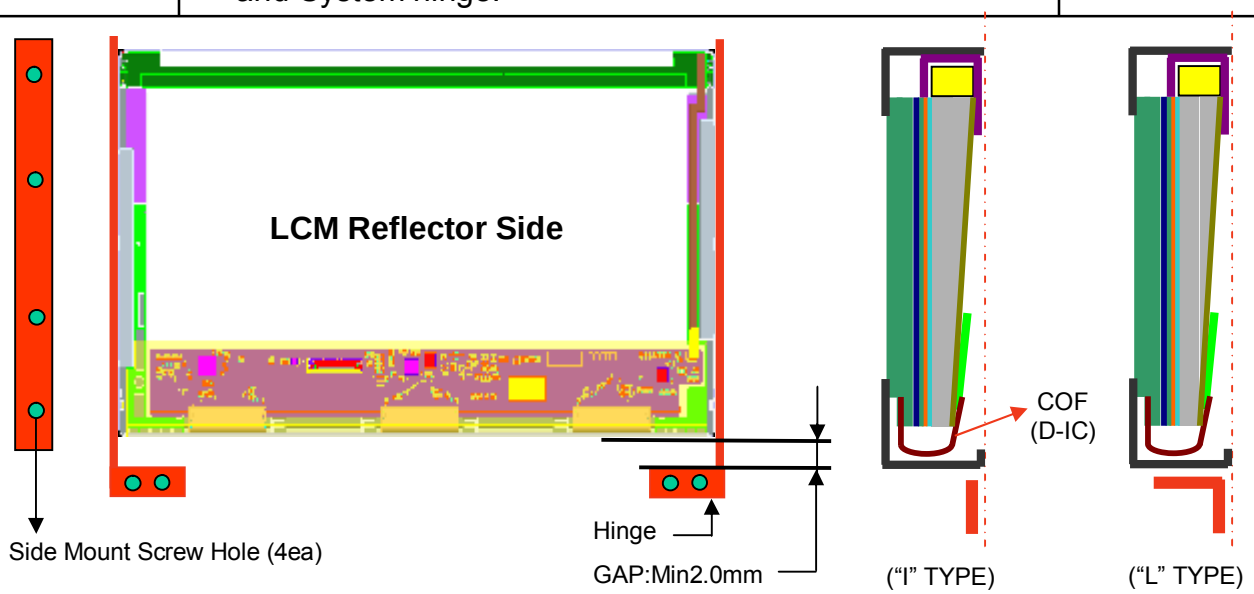


NO GOOD GOOD

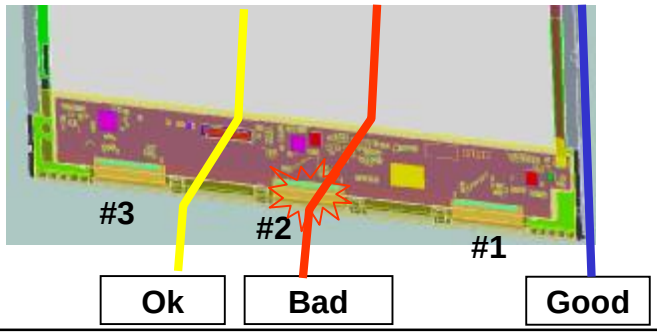
Notes	1.If system antenna is overlapped with T-CON,it might be cause the noise.

LGD Proposal for system cover design.

3	Gap check for securing enough gap between LCM and System hinge.	



Notes	1. At least 2.0mm gap is required to secure from any damage during shock test. 2. "L" type hinge is more recommended than "I" type to get better performance for shock test.
4	Checking the path of the System wire.

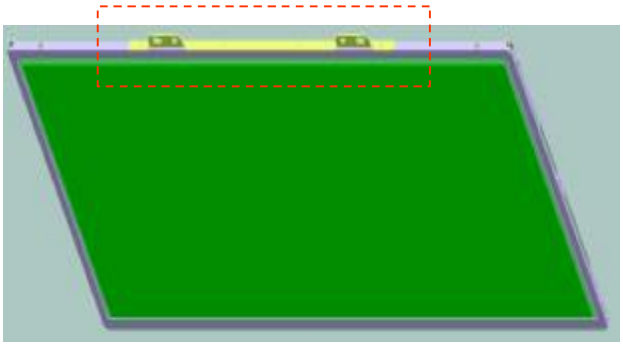


Notes	1. It is required to handle COF area carefully . 2. Good : Wire path does not overlap with LCM OK : Wire path is located between COFs. BAD : Wire path overlapped with COF area. Flat type cable is highly recommended if cable should be located on bad case

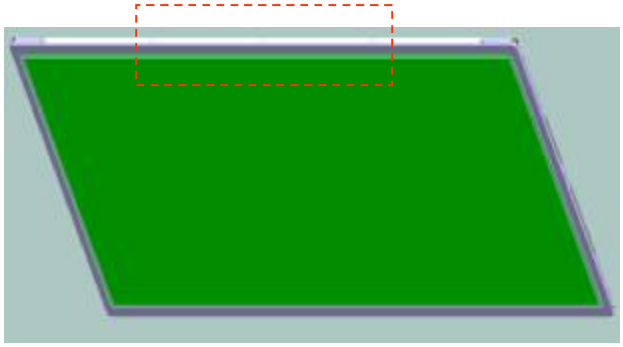
LGD Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

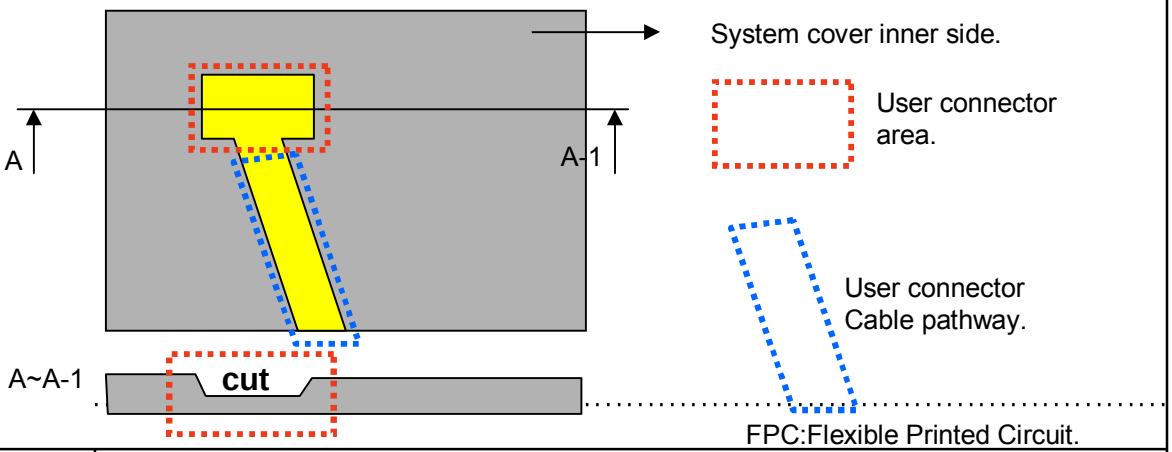


With bracket



Without bracket

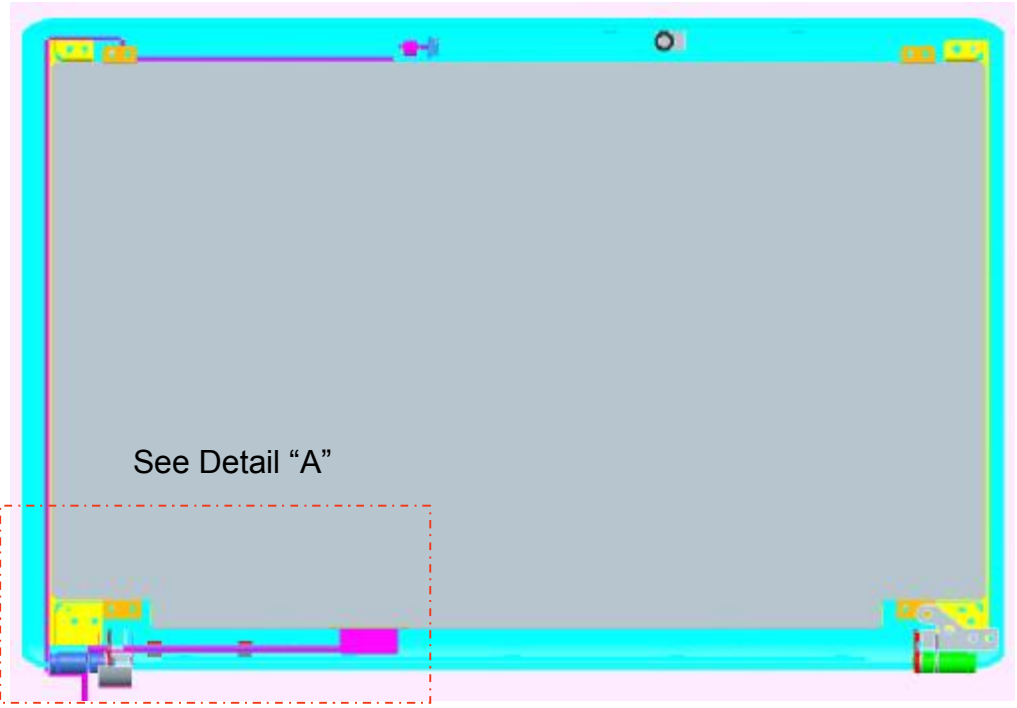
Notes	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..

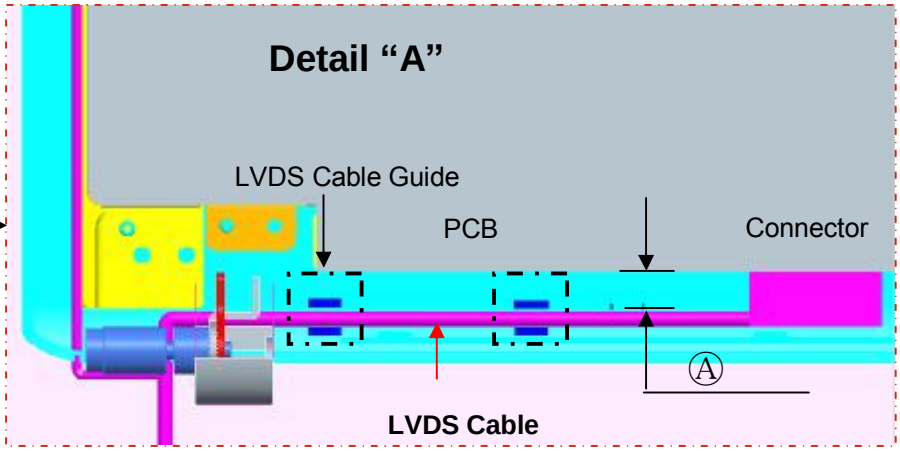


Notes	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

LGD Proposal for system cover design.

7	Checking the path of System LVDS Cable.

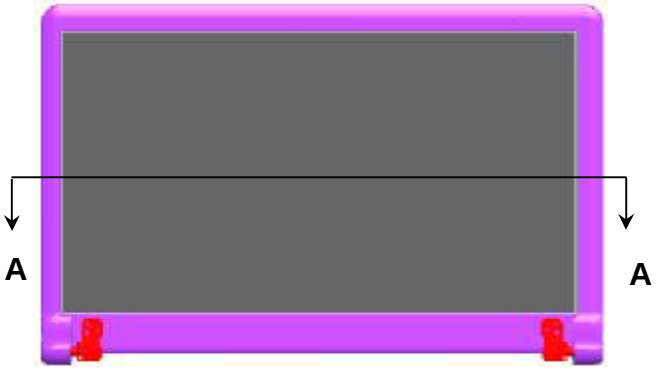


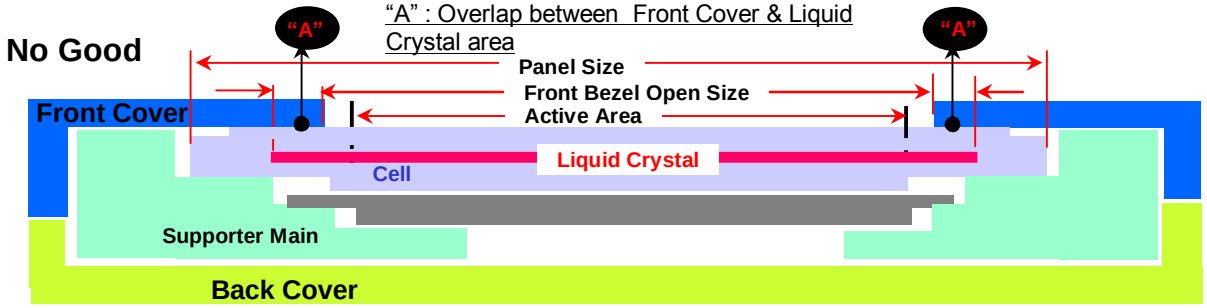


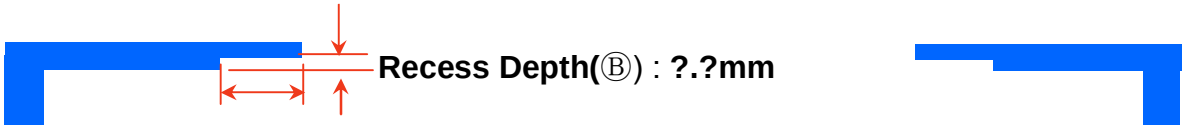
Notes	1. At least 1.0mm gap (Ⓐ) is required to secure from any damage by overlapping system cable and LCM (This overlap may cause a Abnormal Display after hinge test)
	2.”Flat” type of LVDS cable is more recommended than “Cylinderical” type . 3. Making LVDS Cable Guide will give better performance . (Refer to detail “A”)

LGD Proposal for system cover design.

8	Securing additional gap between front cover & LCD at edge of front cover.







Resses Width(Ⓐ) : ?.?mm

※ Recess Width(Ⓐ) : Up / Down /Left /Right
※ Recess Depth(Ⓑ) : Up / Down /Left /Right

Notes	1.Active area which is filled with Liquid Crystal is sensitive against external stress, so additional gap to make recess area on the edge of front cover will be helpful to prevent mechanical Ripple. (Dimension of Recess depends on each model design)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 60950-1, Second Edition, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.

b) CAN/CSA C22.2 No.60950-1-07, Second Edition, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.

c) EN 60950-1:2006 + A11:2009, European Committee for Electrotechnical Standardization (CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

d) IEC 60950-1:2005, Second Edition, The International Electrotechnical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

7-2. EMC

a) ANSI C63.4 “American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz.” American National Standards Institute (ANSI), 2003.

b) CISPR 22 “Information technology equipment – Radio disturbance characteristics – Limit and methods of measurement." International Special Committee on Radio Interference (CISPR), 2005.

c) CISPR 13 “Sound and television broadcast receivers and associated equipment – Radio disturbance characteristics – Limits and method of measurement." International Special Committee on Radio Interference (CISPR), 2006.

7-3. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 20pcs

b) Box Size : 490mm X 390mm X 298mm

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.
(10) When handling the LCD module, it needs to handle with care not to give mechanical stress to the PCB and Mounting Hole area."

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	00	Header	00	00000000
	1	01	Header	FF	11111111
	2	02	Header	FF	11111111
	3	03	Header	FF	11111111
	4	04	Header	FF	11111111
	5	05	Header	FF	11111111
	6	06	Header	FF	11111111
	7	07	Header	00	00000000
Vendor / Product EDID Version	8	08	ID Manufacture Name LGD	30	00110000
	9	09	ID Manufacture Name	E4	11100100
	10	0A	ID Product Code 02C4h	C4	11000100
	11	0B	(Hex. LSB first)	02	00000010
	12	0C	ID Serial No. - Optional ("00h" if not used, Number Only and LSB First)	00	00000000
	13	0D	ID Serial No. - Optional ("00h" if not used, Number Only and LSB First)	00	00000000
	14	0E	ID Serial No. - Optional ("00h" if not used, Number Only and LSB First)	00	00000000
	15	0F	ID Serial No. - Optional ("00h" if not used, Number Only and LSB First)	00	00000000
	16	10	Week of Manufacture - Optional 00 weeks	00	00000000
	17	11	Year of Manufacture 2010 years	14	00010100
	18	12	EDID structure version # = 1	01	00000001
	19	13	EDID revision # = 4	04	00000100
Display Parameters	20	14	Video input Definition = Input is a Digital Video signal Interface , Color Bit Depth : 6 Bits per Primary Color , Digital Video Interface Standard Supported : DisplayPort is supported	95	10010101
	21	15	Horizontal Screen Size (Rounded cm) = 38 cm	26	00100110
	22	16	Vertical Screen Size (Rounded cm) = 21 cm	15	00010101
	23	17	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120 = 2.2 Gamma	78	01111000
	24	18	Feature Support (Display Power Management(DPM) : Standby Mode is not supported, Suspend Mode is not supported, Active Off = Very Low Power is not supported, Supported Color Encoding Formats : RGB 4:4:4 ,Other Feature Support Flags : No_sRGB, Preferred Timing Mode, No_Display is continuous frequency (Multi-mode : Based on EDID's Refresh Rate Block)	02	00000010
Panel Color Coordinates	25	19	Red/Green Low Bits (RxRy/GxGy)	00	00000000
	26	1A	Blue/White Low Bits (BxBy/WxWy)	05	00000101
	27	1B	Red X Rx = 00	00	00000000
	28	1C	Red Y Ry = 00	00	00000000
	29	1D	Green X Gx = 00	00	00000000
	30	1E	Green Y Gy = 00	00	00000000
	31	1F	Blue X Bx = 00	00	00000000
	32	20	Blue Y By = 00	00	00000000
	33	21	White X Wx = 0.313	50	01010000
	34	22	White Y Wy = 0.329	54	01010100
Established Timings	35	23	Established Timing I (00h if not used)	00	00000000
	36	24	Established Timing II (00h if not used)	00	00000000
	37	25	Manufacturer's Timings (00h if not used)	00	00000000
Standard Timing ID	38	26	Standard timing ID1 (Optional, 01h if not used)	01	00000001
	39	27	Standard timing ID1 (Optional, 01h if not used)	01	00000001
	40	28	Standard timing ID2 (Optional, 01h if not used)	01	00000001
	41	29	Standard timing ID2 (Optional, 01h if not used)	01	00000001
	42	2A	Standard timing ID3 (Optional, 01h if not used)	01	00000001
	43	2B	Standard timing ID3 (Optional, 01h if not used)	01	00000001
	44	2C	Standard timing ID4 (Optional, 01h if not used)	01	00000001
	45	2D	Standard timing ID4 (Optional, 01h if not used)	01	00000001
	46	2E	Standard timing ID5 (Optional, 01h if not used)	01	00000001
	47	2F	Standard timing ID5 (Optional, 01h if not used)	01	00000001
	48	30	Standard timing ID6 (Optional, 01h if not used)	01	00000001
	49	31	Standard timing ID6 (Optional, 01h if not used)	01	00000001
	50	32	Standard timing ID7 (Optional, 01h if not used)	01	00000001
	51	33	Standard timing ID7 (Optional, 01h if not used)	01	00000001
	52	34	Standard timing ID8 (Optional, 01h if not used)	01	00000001
	53	35	Standard timing ID8 (Optional, 01h if not used)	01	00000001

Will be updated

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Not fixed	54	36	Pixel Clock/10,000 (LSB)	02	00000010
	55	37	Pixel Clock/10,000 (MSB)	3A	00111010
	56	38	Horizontal Active (lower 8 bits)	80	10000000
	57	39	Horizontal Blanking (Typ-HA) (lower 8 bits)	18	00011000
	58	3A	Horizontal Active / Horizontal Blanking (Typ-HA) (upper 4/4bits)	71	01110001
	59	3B	Vertical Active	38	00111000
	60	3C	Vertical Blanking (Typ-HA) (DE blanking typ for DE only panels)	2D	00101101
	61	3D	Vertical Active : Vertical Blanking (Typ-HA) (upper 4/4bit)	40	01000000
	62	3E	Horizontal Sync. Offset (Typ)	58	01011000
	63	3F	Horizontal Sync. Pulse Width (Typ-HA)	2C	00101100
	64	40	Vertical Sync. Offset (Typ) : Sync Width (Typ-HA)	45	01000101
	65	41	Horizontal / Vertical Sync. Offset / Width (upper 2bits)	00	00000000
	66	42	Horizontal Image Size (mm)	7F	01111110
	67	43	Vertical Image Size (mm)	D7	11010111
	68	44	Horizontal Image Size / Vertical Image Size	10	00010000
	69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	71	47	Non-Interlace, Normal display, no stereo, Digital Separate (Vsync_NEG, Hsync_NEG (outside of V-sync))	19	00011001
Not fixed	72	48	Pixel Clock/10,000 (LSB)	D3	11010011
	73	49	Pixel Clock/10,000 (MSB)	9A	10011010
	74	4A	Horizontal Active (lower 8 bits)	80	10000000
	75	4B	Horizontal Blanking (Typ-HA) (lower 8 bits)	A0	10100000
	76	4C	Horizontal Active / Horizontal Blanking (Typ-HA) (upper 4/4bits)	70	01110000
	77	4D	Vertical Active	38	00111000
	78	4E	Vertical Blanking (Typ-HA) (DE blanking typ for DE only panels)	1F	00011111
	79	4F	Vertical Active : Vertical Blanking (Typ-HA) (upper 4/4bit)	40	01000000
	80	50	Horizontal Sync. Offset (Typ)	14	00010100
	81	51	Horizontal Sync. Pulse Width (Typ-HA)	14	00010100
	82	52	Vertical Sync. Offset (Typ) : Sync Width (Typ-HA)	35	00110101
	83	53	Horizontal / Vertical Sync. Offset / Width (upper 2bits)	00	00000000
	84	54	Horizontal Image Size (mm)	7E	01111110
	85	55	Vertical Image Size (mm)	D7	11010111
	86	56	Horizontal Image Size / Vertical Image Size	10	00010000
	87	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	88	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	89	59	Non-Interlace, Normal display, no stereo, Digital Separate (Vsync_NEG, Hsync_NEG (outside of V-sync))	19	00011001
Timing Descriptor #3	90	5A	Flag: 0x000000	00	00000000
	91	5B	Flag: 0x000000	00	00000000
	92	5C	Flag: 0x000000	00	00000000
	93	5D	Flag: 0x000000	00	00000000
	94	5E	Flag: 0x000000	00	00000000
	95	5F	Flag: 0x000000	00	00000000
	96	60	Flag: 0x000000	00	00000000
	97	61	Flag: 0x000000	00	00000000
	98	62	Flag: 0x000000	00	00000000
	99	63	Flag: 0x000000	00	00000000
	100	64	Flag: 0x000000	00	00000000
	101	65	Flag: 0x000000	00	00000000
	102	66	Flag: 0x000000	00	00000000
	103	67	Flag: 0x000000	00	00000000
	104	68	Flag: 0x000000	00	00000000
	105	69	Flag: 0x000000	00	00000000
	106	6A	Flag: 0x000000	00	00000000
	107	6B	Flag: 0x000000	00	00000000

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments		Value (Hex)	Value (Bin)
Timing Descriptor #4	108	6C	Detailed Timing Descriptions #4		00	00000000
	109	6D	Flag		00	[illegible]
	110	6E	Reserved		00	00000000
	111	6F	[illegible] Brightness Tabl[illegible]		02	00000010
	112	70	Flag		00	00000000
	113	71	PWM % [illegible] @ Ste[illegible]	5 % @ [illegible]	0C	00001100
	114	72	PWM % [illegible] @ Ste[illegible]	[illegible] @ 50 [illegible]	00	00000000
	115	73	PWM % [illegible] @ St[illegible]	[illegible] @ [illegible]	EA	[illegible]
	116	74	Nits [7:0] @ Step 0		00	[illegible]
	117	75	Nits [7:0] @ Step 5		3C	00111100
	118	76	Nits [7:0] @ Step 10		00	00000000
	119	77	Panel Electronics Po[illegible]		00	00000000
	120	78	Backlight Power @ [illegible]		00	00000000
	121	79	Backlight Power @ [illegible]		00	00000000
	122	7A	[illegible] @ [illegible] PWM		00	00000000
	123	7B	Flag		00	00000000
	124	7C	Flag		00	00000000
	125	7D	Flag		00	00000000
Chec[k]	126	7E	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)		00	00000000
	127	7F	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)		5F	[illegible]

Will be updated