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Engineering Specification

Type 12.1 XGA Color TFT/LCD Module
Model Name:IAXG01

Document Control Number : OEM I-901-03

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Product Development
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
February 7,2001	OEM901-01	All	First Edition for customer. Based on Internal Spec. as of January 29,2001.
February 26,2001	OEM901-02	1,5 1,5,6,7 26,27	The Model Name was changed to IAXG01 based on Internal memo on February 23,2001. To avoid "inch" indication. To update Reference Drawings.
August 7,2001	OEM901-03	 6 9 14-17 18 21 22 23 25 29	Besed on Internal Spec. EC H30851 as of June 18,2001. To update Power Consumption. To update Color Chromaticity. To update Interface Signal Electrical Characteristics. To add Recommended Guidelines for Motherboard PCB Design and Cable Selection. To update Parameter guide line for CFL Inverter. To update Luminance versus Lamp Current. To add Note for Timing Characteristics. To update Typ. value of PDD and IDD. To update Conditions of Acceptability.
January 15,2002	OEM I-901-03		Updated by establishment of the New Company as "International Display Technology".

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950). Do not connect the CFL in Hazardous Voltage Circuit.
15) Gently wipe the covers and the screen with a soft cloth.
16) Remove finger marks and grease with a damp cloth and mild detergent; do not use solvents or abrasives.
17) Never apply detergent or other liquid directly to the screen. Dampen the cloth and then wipe.

- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by International Display Technology for any infringements of patents or other right of the third partied which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of International Display Technology or others.
- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporationg this product.

2.0 General Description

This specification applies to the Type 12.1 Color TFT/LCD Module 'IAXG01'.
This module is designed for a display unit of notebook style personal computer.
The screen format and electrical interface are intended to support the XGA(1024(H) x 768(V)) screen.
Support color is native 262K colors(RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

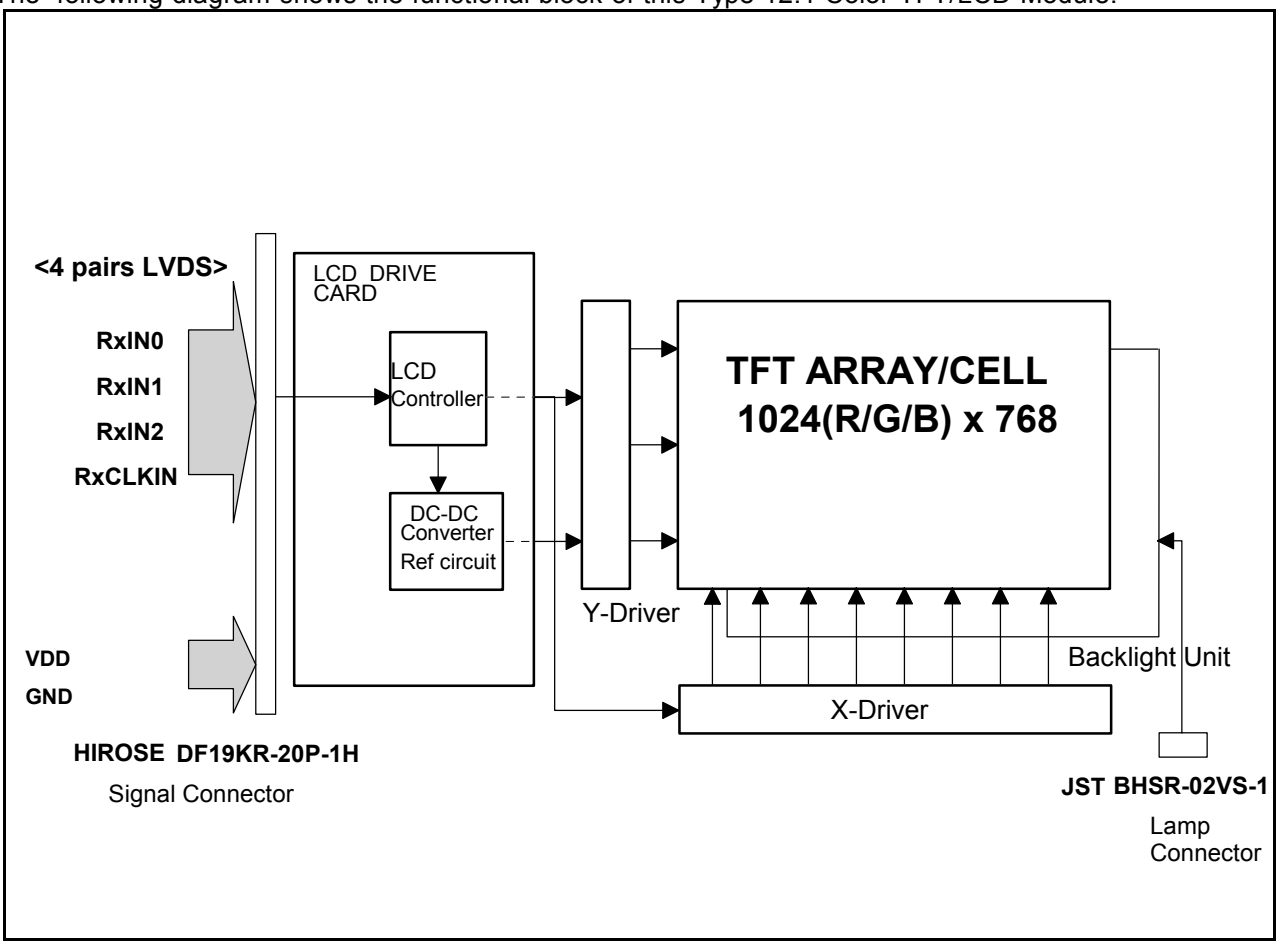
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	307
Pixels H x V	1024(x3) x 768
Active Area [mm]	245.76(H) x 184.32(V)
Pixel Pitch [mm]	0.080(per one triad) x 0.240
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	290 Typ.
Physical Size [mm]	261.0(W) x 198.0(H) x 5.0(D) Typ.
Display Mode	Normally White
Support Color	Native 262K colors(RGB 6-bit data driver)
White Luminance [cd/m^2] Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA)	 95 Typ. (center), 90 Typ. (5 points average) 160 Typ. (center),150 Typ. (5 points average)
Contrast Ratio	250 : 1 Typ.
Optical Rise Time/Fall Time [msec]	30Typ.,50 MAX.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt] (VDD Line) (VCFL Line)	 1.2 Typ. 3.5 Typ.
Electrical Interface	4 pairs, single LVDS
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 12.1 Color TFT/LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Signal Voltage	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+1,500	Vrms	Note 2
CFL Current	ICFL	-	7	mArms	
CFL Peak Inrush Current	ICFLP	-	20	mA	
Operating Temperature	TOP	0	+50	deg.C	Note 1
Operating Relative Humidity	HOP	8	95	%RH	Note 1
Storage Temperature	TST	-20	+60	deg.C	Note 1
Storage Relative Humidity	HST	5	95	%RH	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.
Note 2 : Duration : 50msec Max. Ta=0 degree C

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≥10 (Left) Vertical (Upper) K≥10 (Lower)	40 40 15 30	- - - -
Contrast ratio		250	-
Response Time	Rising	30	50Max
(ms)	Falling	30	50Max
Color	Red x	0.577	-
Chromaticity	Red y	0.338	-
(CIE)	Green x	0.310	-
	Green y	0.554	-
	Blue x	0.158	-
	Blue y	0.124	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2) ICFL 6.5 mA		160Typ. Center 150Typ. 5 points average	

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	DF19KR-20P-1H
Mating Receptacle/Part Number	DF19G-20S-1F (for FPC type connector) DF19G-20S-1C (for Cable type connector)

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Pin#	Signal	Pin#	Signal
1	VDD	11	RxIN2-
2	VDD	12	RxIN2+
3	GND	13	GND
4	GND	14	RxCLKIN-
5	RxIN0-	15	RxCLKIN+
6	RxIN0+	16	GND
7	GND	17	Reserved
8	RxIN1-	18	Reserved
9	RxIN1+	19	GND
10	GND	20	GND

Note:
'Reserved' pins are not allowed to connect any other line.

Voltage levels of all input signals are LVDS compatible (except VDD,). Refer to "Signal Electrical Characteristics for LVDS(*)", for voltage levels of all input signals.

5.3 Interface Signal Description

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Signal Name	Description
RxIN0+, RxIN0-	LVDS differential data input (Red0-Red5, Green0)
RxIN1+, RxIN1-	LVDS differential data input (Green1-Green5,Blue0-Blue1)
RxIN2+, RxIN2-	LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG)
RxCLKIN+, RxCLKIN-	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note:

- The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
- Input signals shall be low or Hi-Z state when VDD is off

SIGNAL NAME	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is strobed at te falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	[mV]	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			[mV]	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	[mV]	
Common Mode Voltage	Vcm	1.0	1.2	1.4	[V]	Vth - Vtl = 200mV
Common Mode Voltage Offset	△Vcm	-50		+50	[mV]	Vth - Vtl = 200mV

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure **Measurement system**).

Voltage Definitions

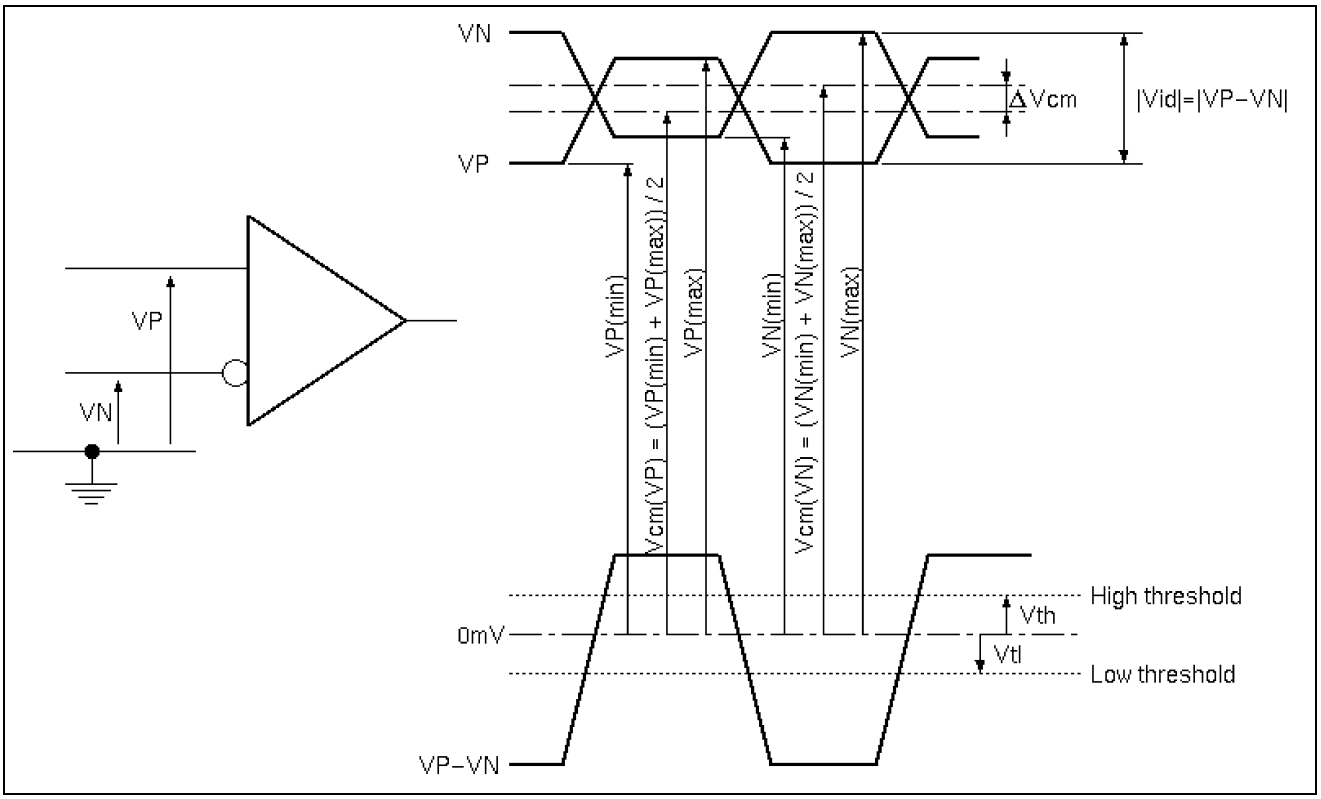


Figure. Measurement system

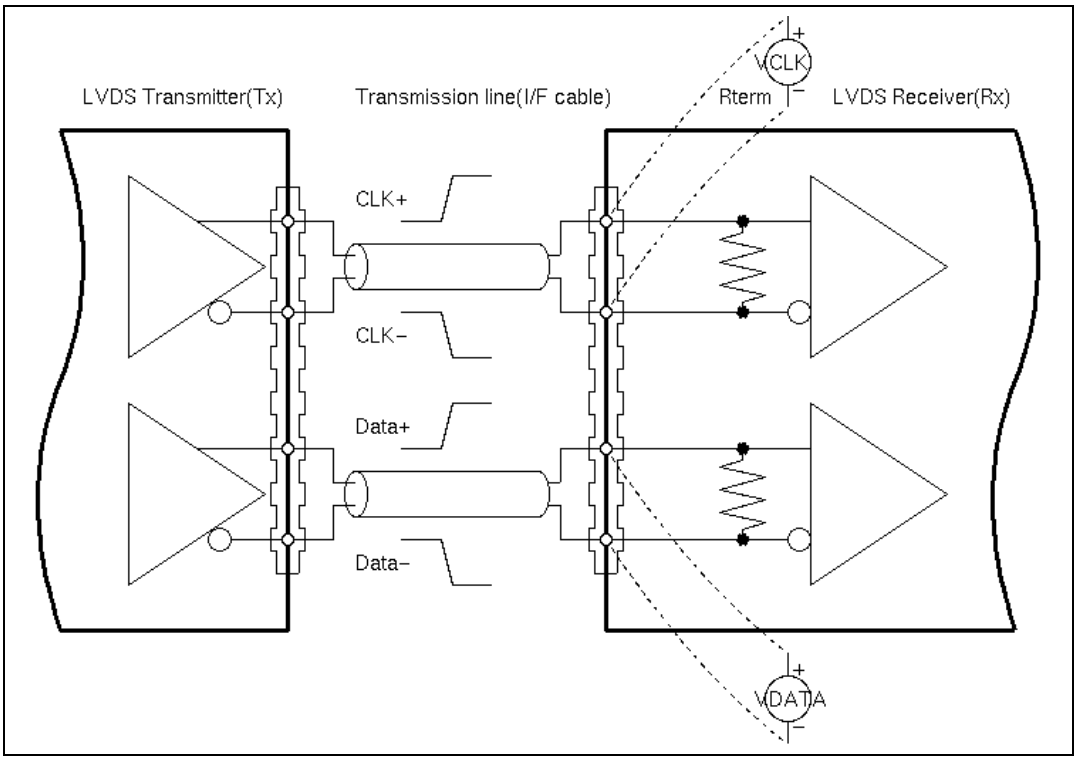


Table. Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	50	65	67	MHz	
Cycle Time	tc	14.93	15.38	20.00	ns	
Data Setup Time(Note 1)	Tsu	600			ps	fc = 65MHz, tCCJ < 50ps, Vth-Vtl = 200mV, Vcm = 1.2V, △Vcm = 0
Data Hold Time(Note 2)	Thd	600			ps	
Cycle-to-cycle jitter(Note 3)	tCCJ	-150		+150	ps	fc = 65MHz, Tsu=Thd=900ps
Cycle Modulation Rate(Note 4)	tCJavg			20	ps/clk	fc = 65MHz, Tsu=Thd=900ps

Note 1: All values are at VDD=3.3V, Ta=25 degree C.

Note 2: See figure **"Timing Definition"** and **"Timing Definition(detail A)"** for definition.

Note 3: Jitter is the magnitude of the change in input clock period.

Note 4: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles.
This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Figure. Timing Definition

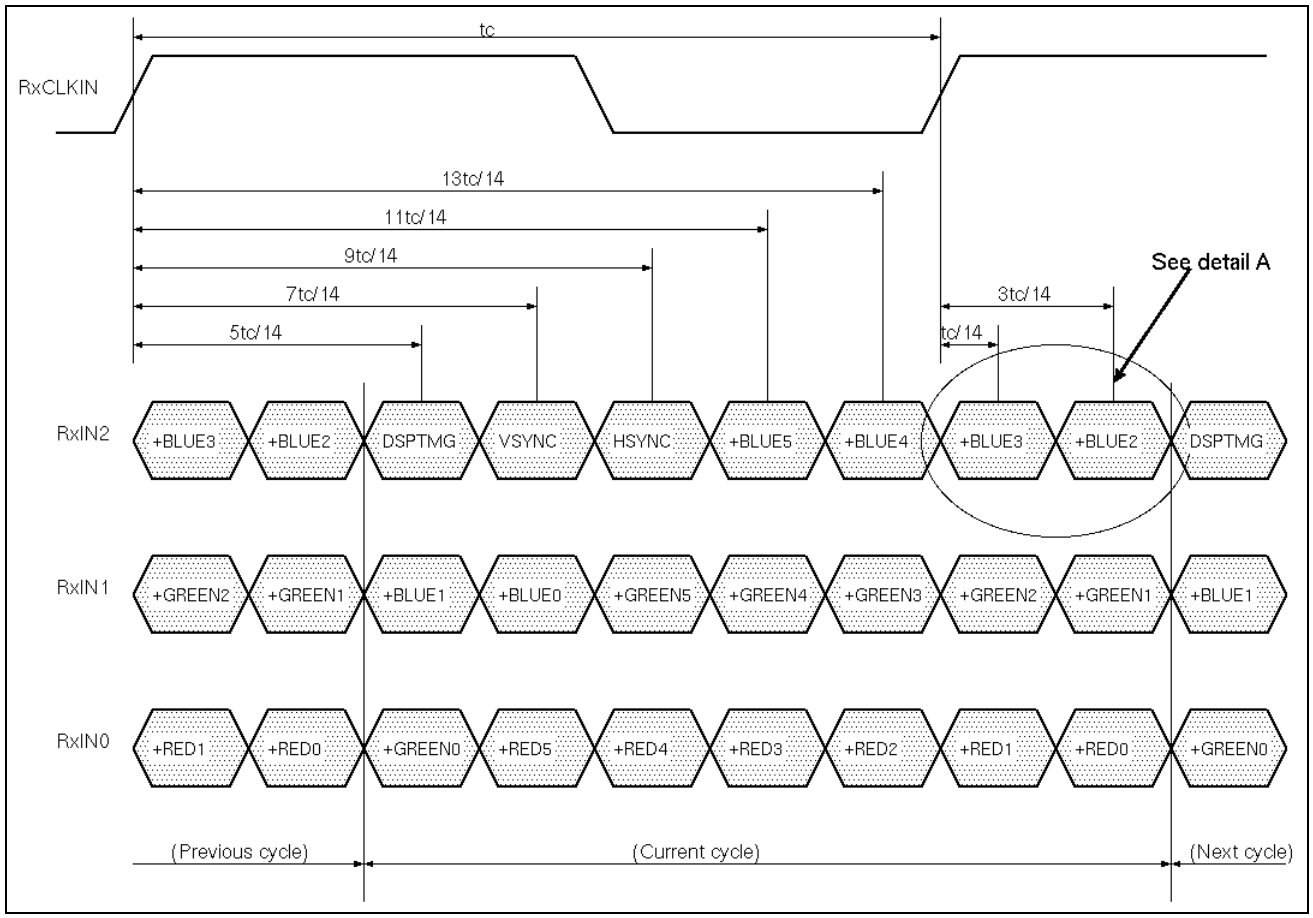
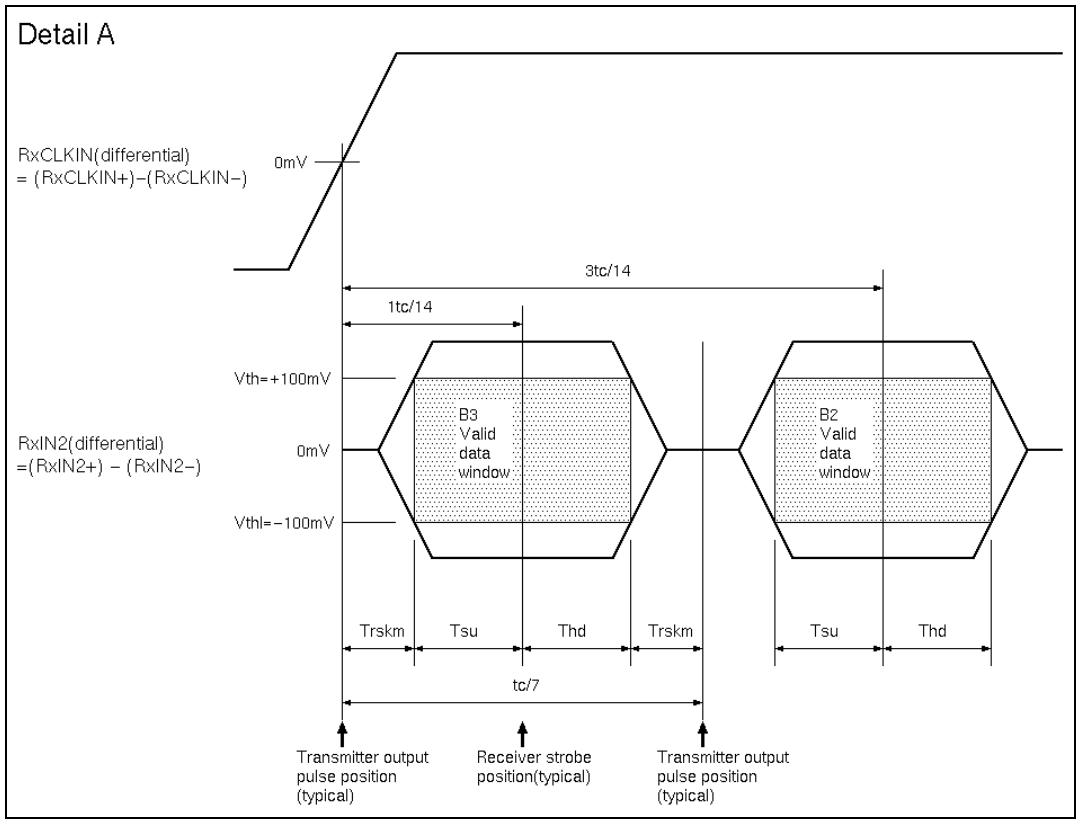


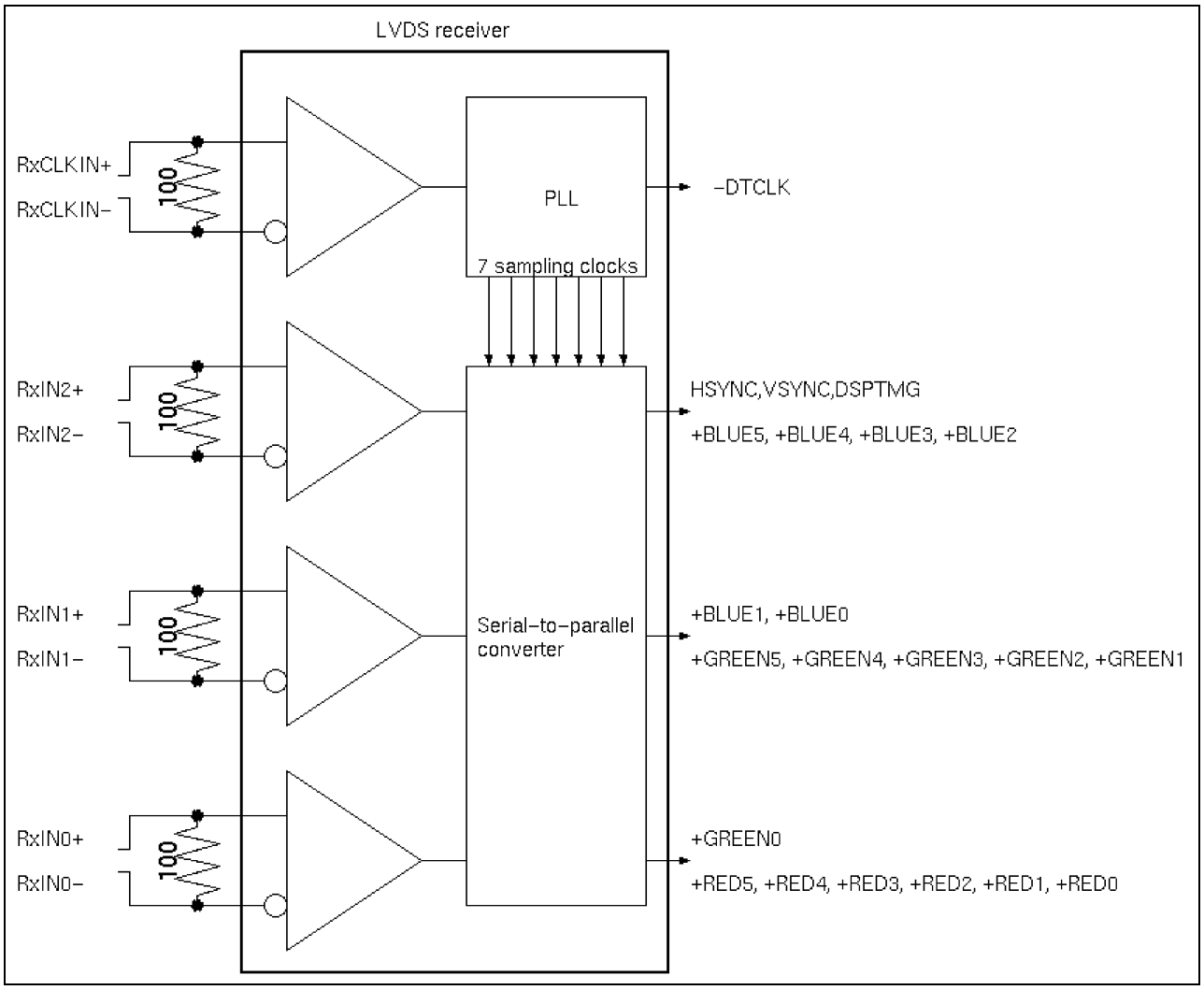
Figure. Timing Definition(detail A)



Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

5.4.2 LVDS Receiver Internal Circuit

Internal circuit of LVDS inputs are as follows.



.The module uses a 100ohm resistor between positive and negative data lines of each receiver input.

5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

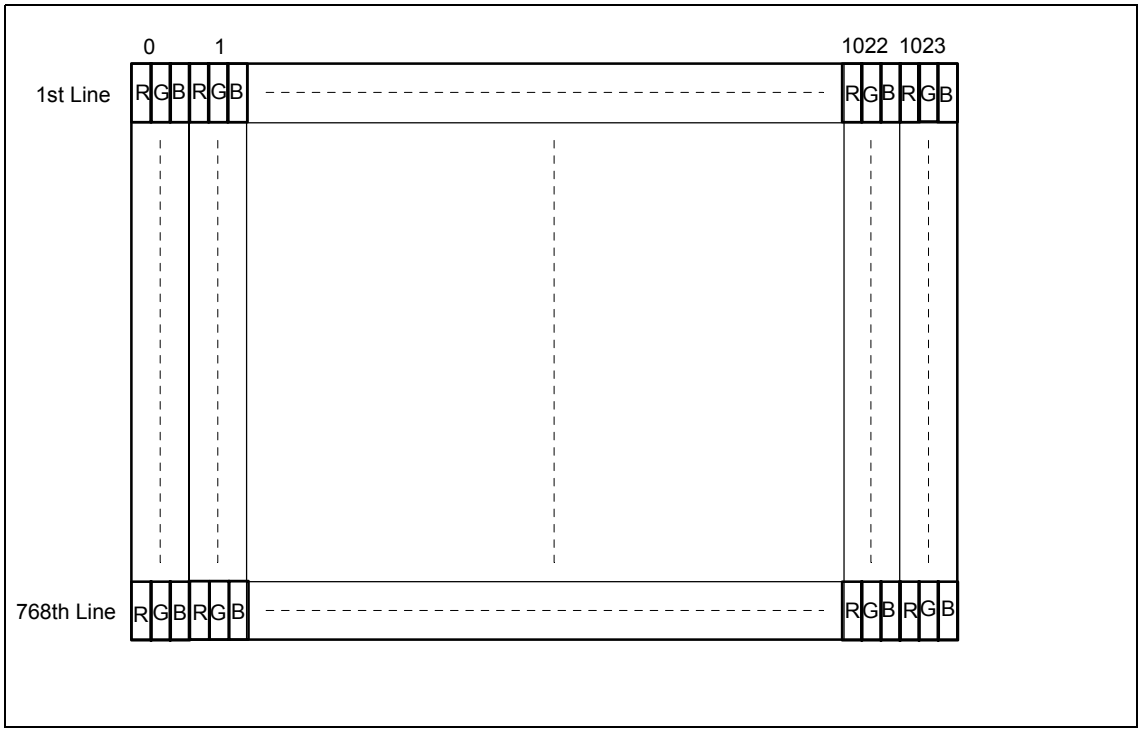
- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.



7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	DP-1	DP-2	MAX	UNITS	CONDITION
White Luminance (Center) (5 Points average)	 - -	 95 90	 160 150	 - -	cd/m^2	(Ta=25 deg.C)
CFL current(ICFL)	3.0	3.5	6.5	7.0	mArms	(Ta=25 deg.C)
CFL Frequency(FCFL)	40			60	KHz	(Ta=25 deg.C) **Note 1**
CFL Ignition Voltage(Vs)	1,400	-	-	-	Vrms	(Ta= 0 deg.C) **Note 3**
CFL Voltage (Reference)(VCFL)	-	655	550	-	Vrms	(Ta=25 deg.C) **Note 2**
CFL Power consumption(PCFL)	-	2.3	3.6	-	W	(Ta=25 deg.C) **Note 2**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 4: DP-1 and DP-2 are recommended Design Points.

*1 All of characteristics listed are measured under the condition using the Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

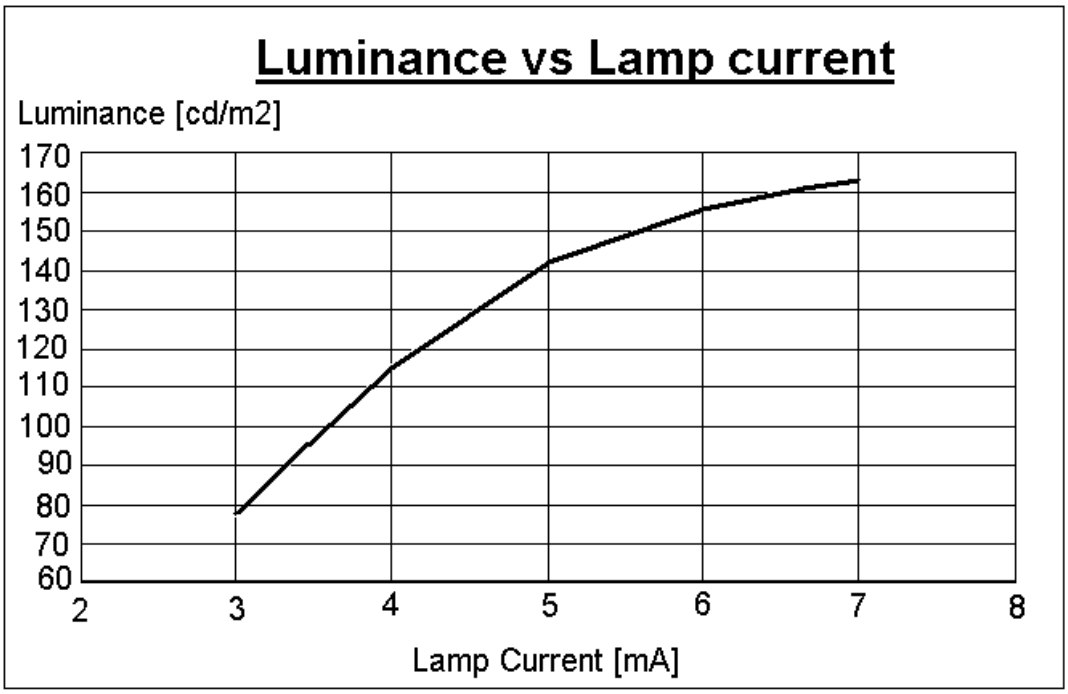
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

*7 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4[mA].

The following chart is Luminance versus Lamp current for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

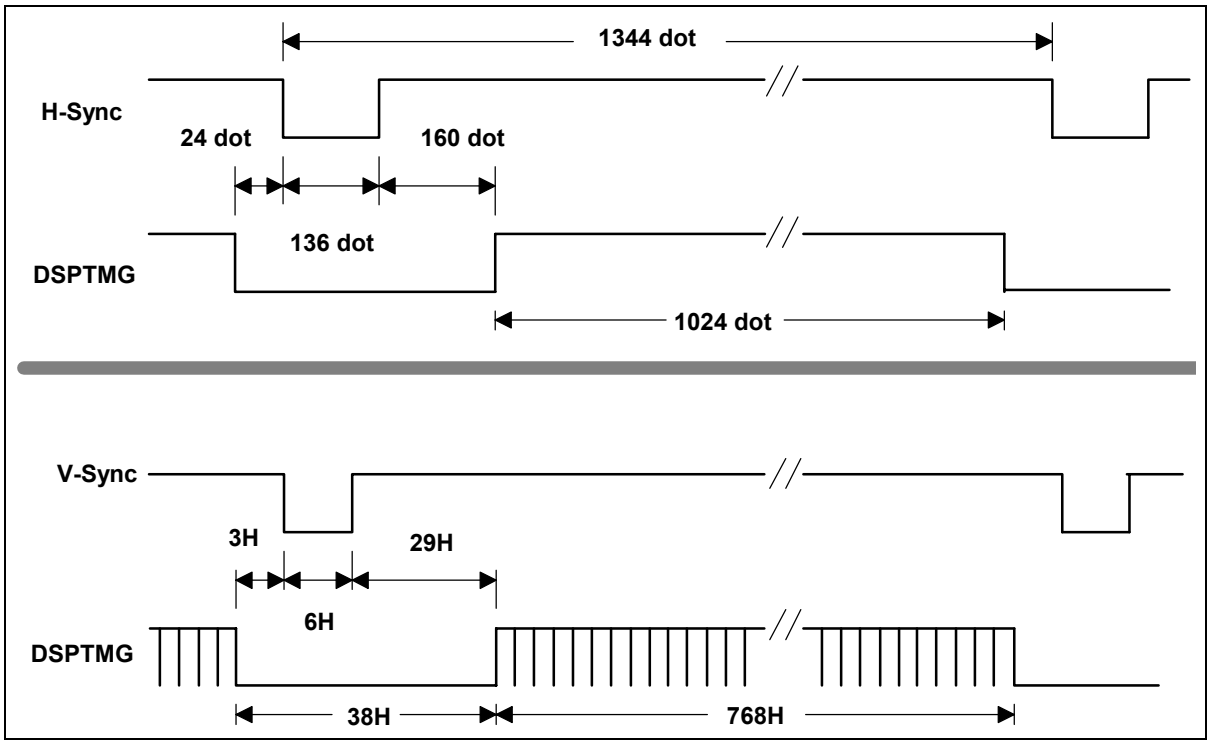
8.1 Timing Characteristics

Symbol		MIN	TYP	MAX	Unit	Note
fdck	DTCLK Frequency	50.00	65.00	67.00	MHz	
tck	DTCLK cycle time	14.93	15.38	20.00	nsec	
tx	X total time	1206	1344	2047	tck	
tacx	X active time	1024	1024	1024	tck	
tbkx	X blank time	90	320		tck	1
Hsync	H frequency		48.363		KHz	
Hsw	H-Sync width	2	136		tck	2
Hbp	H back porch	1	160		tck	2
Hfp	H front porch	0	24		tck	
ty	Y total time	777	806	1023	tx	
tacy	Y active time	768	768	768	tx	
Vsync	Frame rate	(55)	60	61	Hz	
Vw	V-sync Width	1	6		tx	
Vfp	V-sync front porch	1	3		tx	
Vbp	V-sync back porch	7	29	63	tx	3

Note 1 : 1. tbkx=Hfp+Hsw+Hbp
2. Hsw + Hbp should be less than 515 [tck].
3. Vbp should be static

Note 2 : When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module protection Mode.

8.2 Timing Definition



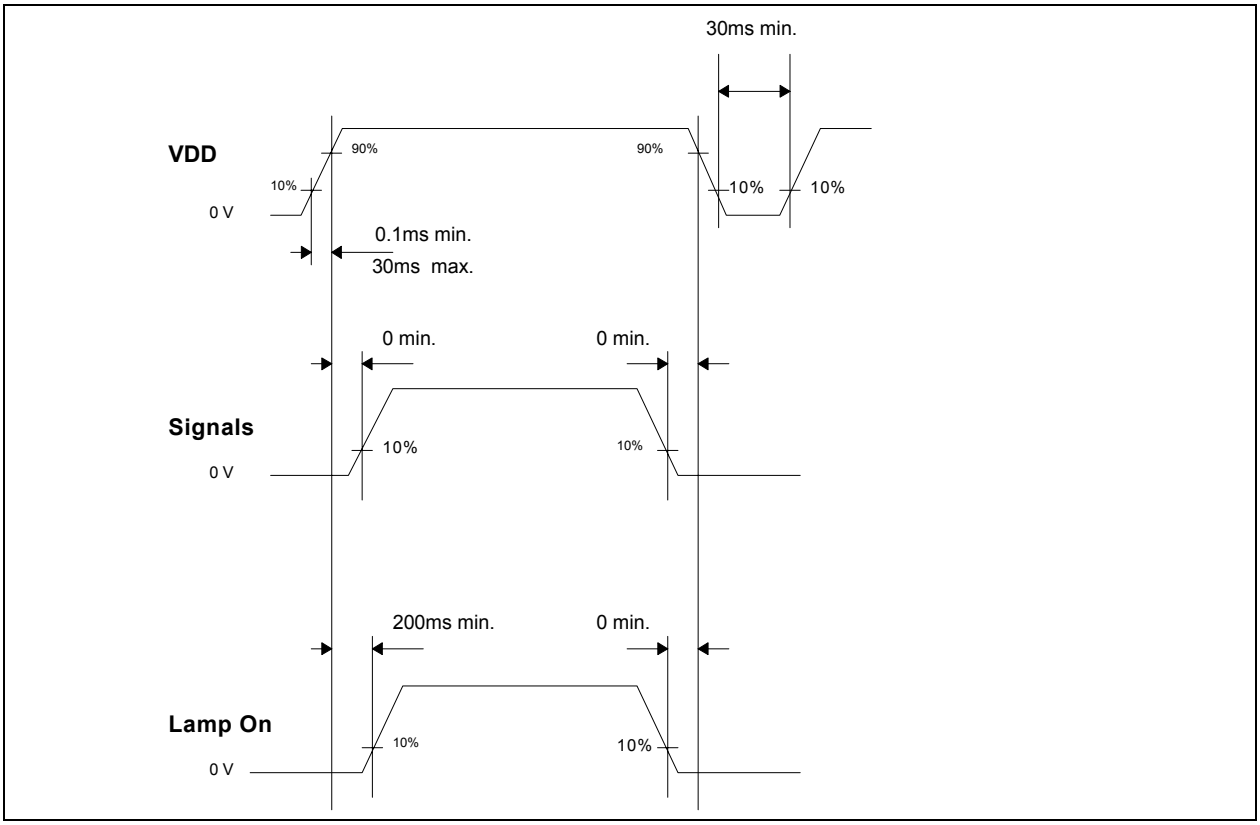
9.0 Power Consumption

Input power specifications are as follows;

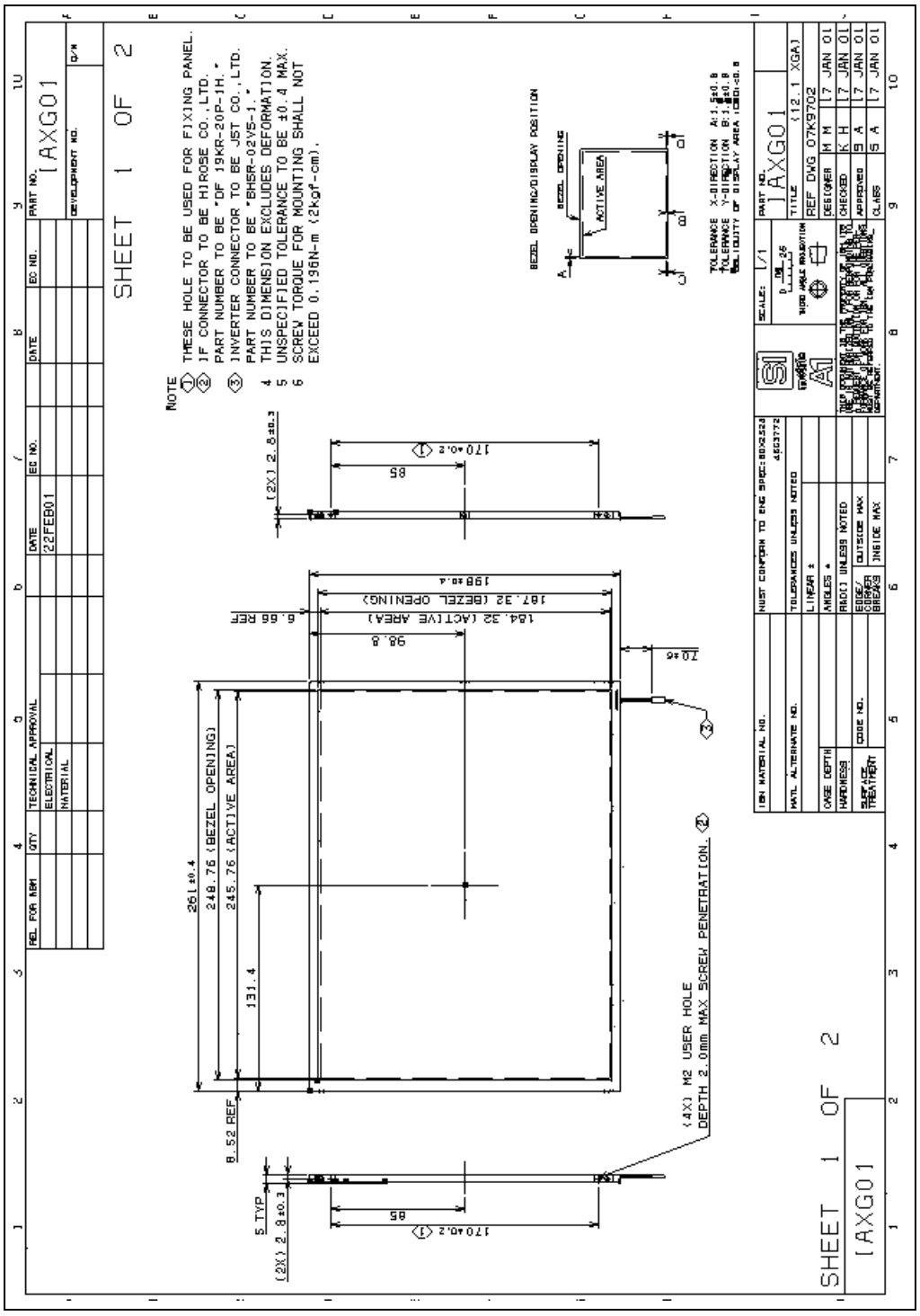
SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 20[uF]
PDD	VDD Power		1.2		[W]	VDD=3.3[V], All Black Pattern,
				1.6	[W]	VDD=3.3[V], Max. Pattern
IDD	VDD Current		360		[mA]	VDD=3.3[V], All Black Pattern
				480	[mA]	VDD=3.3[V], Max Pattern
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	

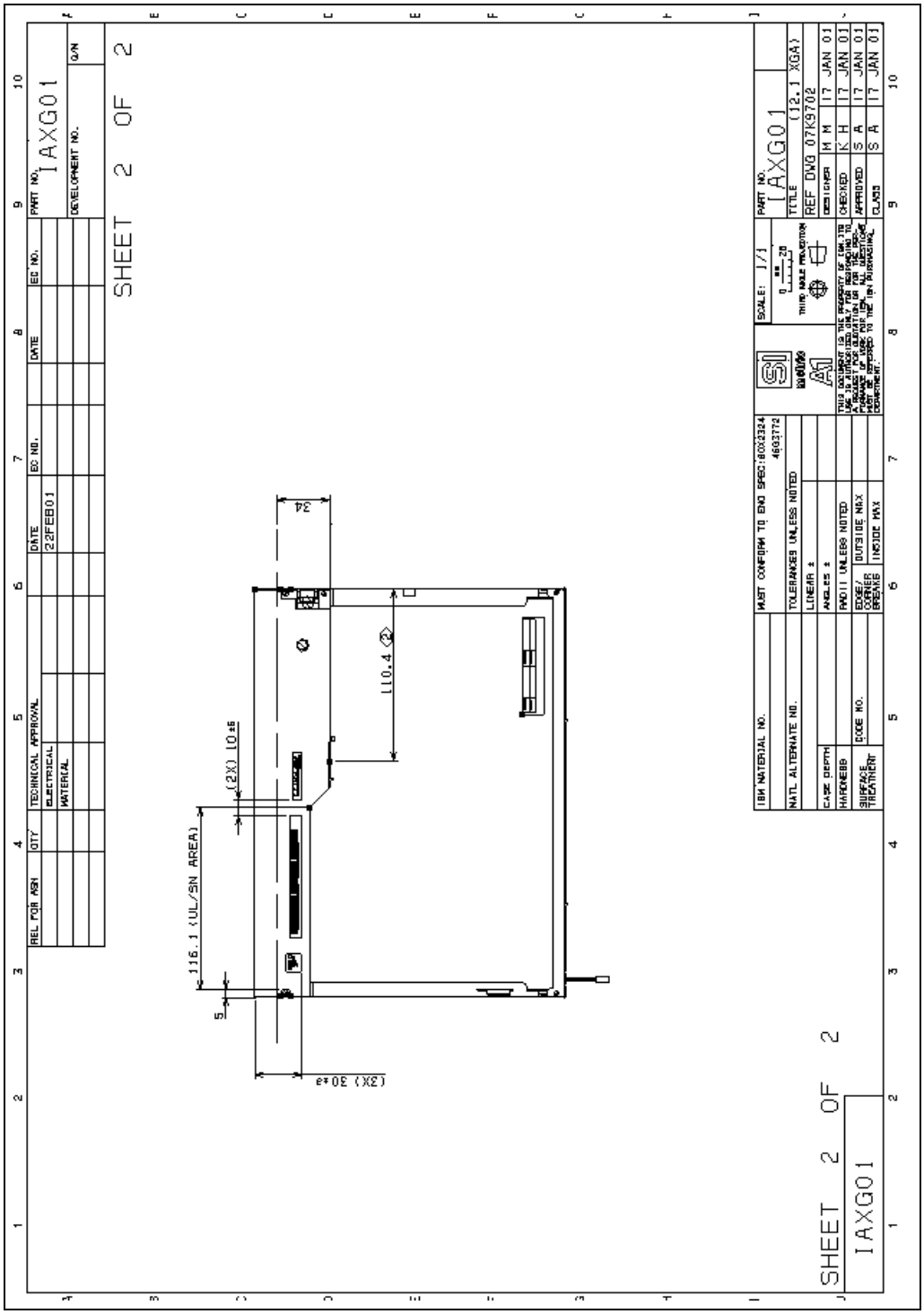
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.60950-00 *UL 60950, Third Edition, including revisions through revision date March 1,1998, which are based on the Fourth Amendment to IEC 60950, Second Edition, which would cover the component itself if submitted for Listing.
- CF Lamp circuit for this model should be supplied from Limited Current Circuit.
- The units are supplied by Limited Power Sources.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.
- Panel back should be separated form source of fire at least 13mm of air or solid barrier of material of Flammability V-1 or less flammable.

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