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Chunghwa Picture Tubes, Ltd.
Product Specification

To :
Date :

TFT LCD
CLAA080WK05 XN

ACCEPTED BY : (V0.4)

APPROVED BY	CHECKED BY	PREPARED BY

Prepared by :
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REVISION STATUS

Revision Notice	Description	Page	Rev. Date
Ver. 0.0	First revision (Tentative)	-	2014.12.11
Ver. 0.1	3.1 TFT LCD	6	2015.05.29
Ver. 0.1	3.2 TFT-LCD Current Consumption	7	2015.05.29
Ver. 0.2	7. optical characteristics	17	2015.06.25
Ver. 0.3	7. optical characteristics	17	2015.07.17
Ver. 0.4	3.1 TFT LCD	6~7	2015.09.01
Ver. 0.4	3.2 TFT-LCD Current Consumption	8	2015.09.01
Ver. 0.4	5.1 Timing Specification	14	2015.09.01

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1. OVERVIEW

CLAA080WK05 XN is 8” color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs ,control circuit and LED backlight. By applying 1280×720 images are displayed on the 8” diagonal screen. Display 16.7M colors by R.G.B signal input.

General specification are summarized in the following table:

ITEM	SPECIFICATION			
Display Area (mm)	177.024(H)×99.576(V)			
Number of Pixels	1280(H) × 3 (RGB) × 720(V)			
Pixel Pitch (mm)	0.1383(W) x 0.1383(H)			
Color Pixel Arrangement	RGB vertical stripe			
Display Mode	Normally Black			
Number of Colors	16.7M (6bit+2bit HiFRC)			
Brightness (cd/m^2)	**500(typ)**			
Response Time (ms)	25(typ)			
Contrast Ratio	900:1(typ)			
Optimum Viewing Direction	Full			
Viewing Angle (CR≧10)	170 degree (Horizontal)			
	170 degree (Vertical)			
Power Consumption (W)	**5.184 W(typ.)(B/L)** , 0.825W(typ.)(LCD)			
Interface connection	LVDS			
Module Size (mm) –(with tape)		Min.	Typ.	Max
	Horizontal (H)	**189.7**	**190**	**190.3**
	Vertical (V)	**119.7**	**120**	**120.3**
	Depth (D) (W/O FPC)	**5.7**	**6**	**6.3**
Module Weight (g)	**TBD (typ.)**			
Backlight Unit	LED			
Surface Treatment	AG 25%,Hardness :3H			

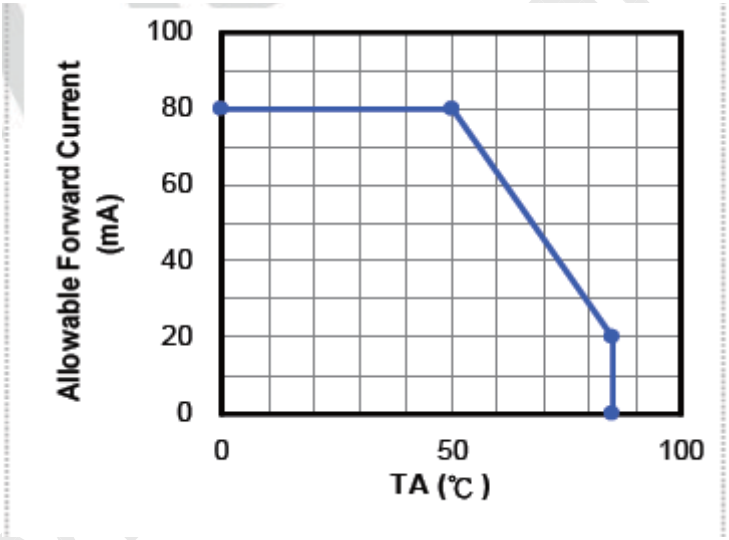
. I S

Th followi g are ma imun v lues hic , if exceede , ma cause faulty op ation or damage to he unit.

I em	Symb l	Min.	x.	nit	Note
owe Supply Voltag For L D	VDD	-0.3	.96	V	
An log Su ply Volta e	VDD	-0 5	4.8	V	
G e On Voltag	VGH	-0.3	40	V	
Gate O f Volta e	V L	- 0	0.	V	
Gate n-Gate Off Vol age	GH-V L	-0.		V	
O era ion em e		20	7	℃	ote1
St rag Te per t			80		Note1
orw rd Curr nt (pe LED	**l**				
se forwar current (pe LE)	**l p**		**40**	**mA**	**Note2**

Note 1】If u ers se he p oduct out off the env ronme tal pe a io r ge (t mperatu e and humid ty), it i l h ve visua quali y co cerns

【N te 】perati g m st nde the conditio as below drawi g.
(Ambient emp rature /Al ow ble orwa d Curr nt) Eac LED .



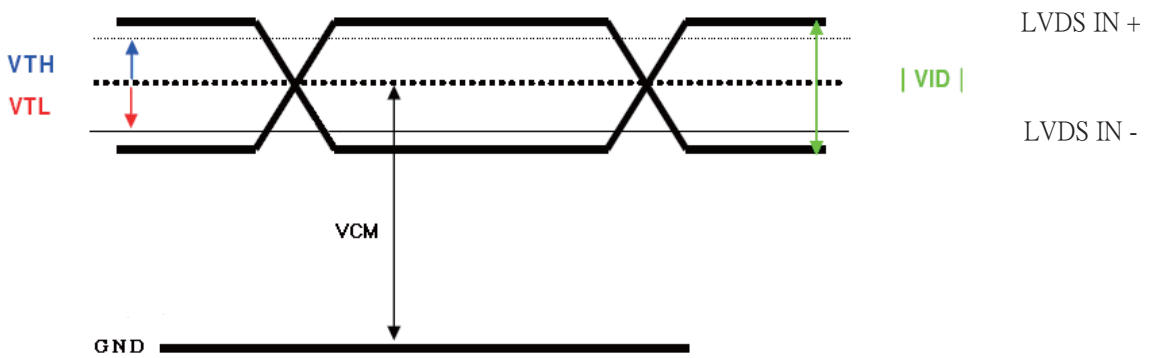
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD

Ta=25℃

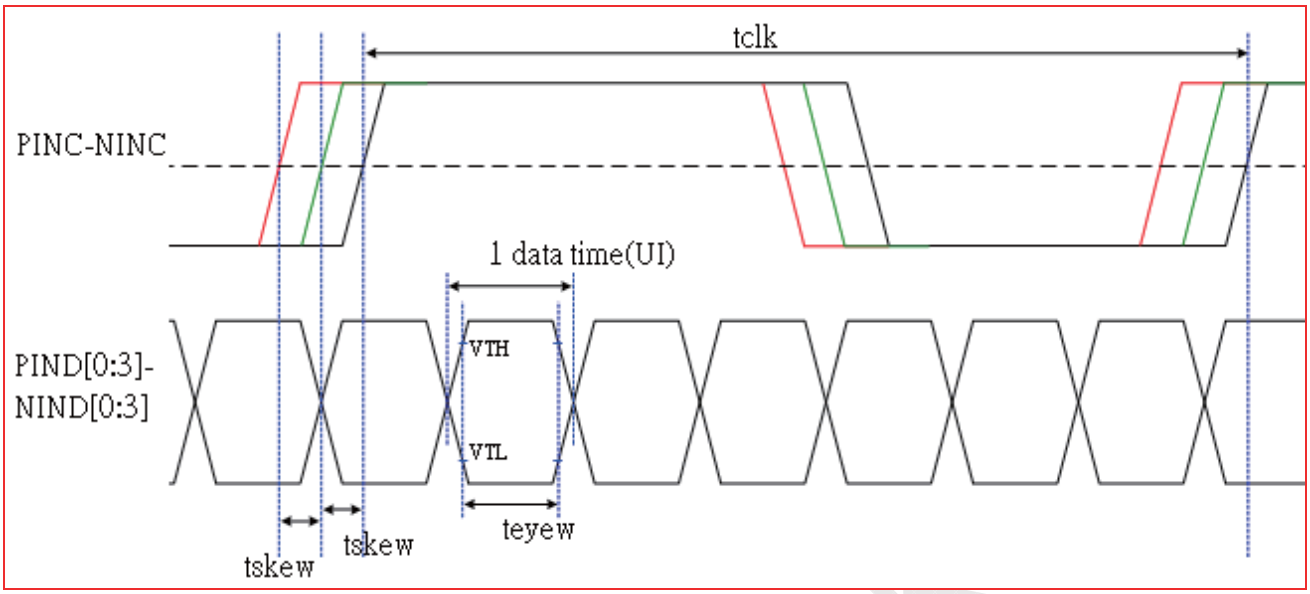
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	DVDD	3	3.3	3.6	V	
Logic Input Voltage (LVDS:IN+,IN-)	VCM	$\frac{\lvert VID \rvert}{2}$	-	$2.4-\frac{\lvert VID \rvert}{2}$	V	Note1
	$\lvert VID \rvert$	200	-	600	mV	Note1
	VTH	-	-	100	mV	VCM=1.2V Note1
	VTL	-100	-	-	mV	
Logic Input Voltage	VIH	0.7*DVDD	-	DVDD	V	
	VIL	GND	-	0.3*DVDD	V	
1 Data time	UI	-	tclk*1/7	-	tclk	Note3
LVDS clock to data skew	tskew	-	-	300	ps	Note3
input data eye width	teyew	1403	-	-	ps	Note3
Analog Power Supply Voltage	AVDD	12.2	12.4	12.6	V	
Gate On Power Supply Voltage	VGH	21	22	23	V	
Gate Off Power Supply Voltage	VGL	-6.6	-6	-5.4	V	
GAMMA Voltage1	V1		12.042		V	Note2
GAMMA Voltage 2	V2		10.858		V	Note2
GAMMA Voltage 3	V3		9.535		V	Note2
GAMMA Voltage 4	V4		8.843		V	Note2
GAMMA Voltage 5	V5		8.261		V	Note2
GAMMA Voltage 6	V6		6.952		V	Note2
GAMMA Voltage 7	V7		6.871		V	Note2
GAMMA Voltage 8	V8		5.875		V	Note2
GAMMA Voltage 9	V9		5.775		V	Note2
GAMMA Voltage 10	V10		4.367		V	Note2
GAMMA Voltage 11	V11		3.797		V	Note2
GAMMA Voltage 12	V12		3.076		V	Note2
GAMMA Voltage 13	V13		1.743		V	Note2
GAMMA Voltage 14	V14		0.238		V	Note2

【Note1】LVDS signal



N a t tag for cus omer, it could e adj st y customer.
2)Th voltage of thes pins must be: AGND .1<V14<V13<V12< 11<V10< 9< 8<0 6AVDD;
0. AV D<V7< 6< 5<V4<V <V <V1< AVDD 0.1

【Note3】 he follo ing ondi on s base on operation frequency at 71.3MHz



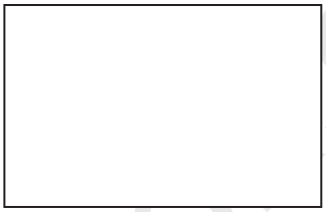
erence voltage for customer.C stomer s d adjust V OM voltag by Vari bl
Res st r to make the flick r evel be nimum.

L o

I		Cond tion	Min	Typ.	Ma .	Unit	Note
Ga e on Current	IVGH	VGH =22V	-	0.5	1	A	【Note1】
Gate off urr nt	IVGL	VGL= -6	-	0.5	1	mA	Note 】
Digi al Curren	IDV D	DV D = .3V	-	36	60	mA	【 ot 1】
Anal g Cu ren	IAV D	AVD 1 .4V	-	3	60	A	【 ote1】
T tal ower Con u pti n	P		-	579	970	mW	Note1】

【Note 】 Ty i al: n er 25 g ay patt rn @67 3MHz
Max m m: Un er White p ttern @67.3 Hz

2 ray pat er



Wh te Patte

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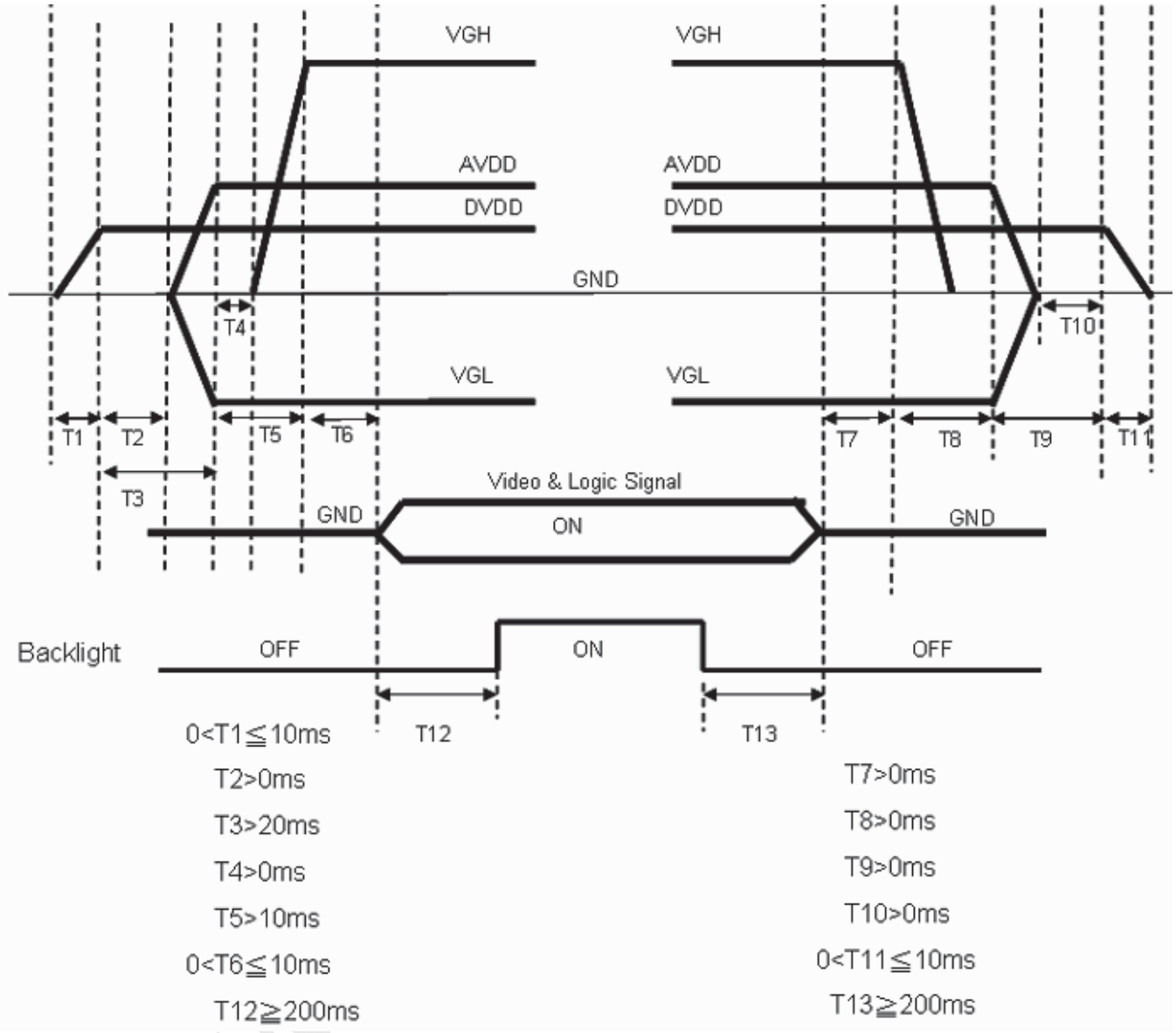
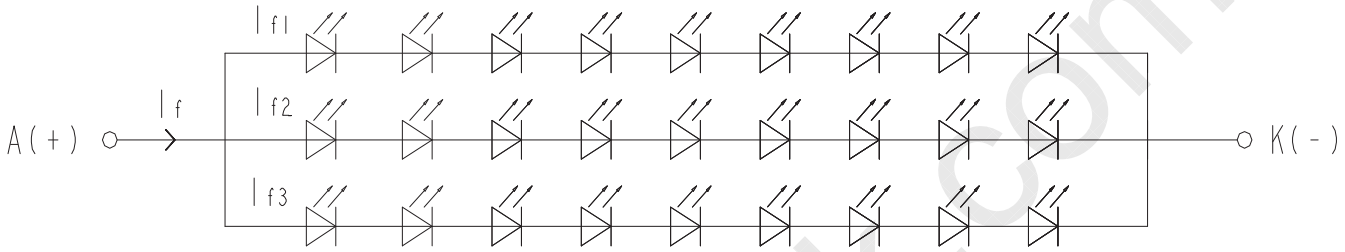
o D→ ide &Logic ignal→Ba klight
Power Off Backlight→Vi eo & ogic Signal→ VGH VDD/VGL→DVDD



g

	O	O	IN	TY	MAX	UNI	NOTE
LE curre t	IL	a=2 ℃ (60mA/ser se)	-	180	--	mA	*1) *
LED voltage	VL	Ta 5℃ 60mA/seri)	26.5	28.	31.05	V	*1) *2)
owe co sum tion	WL	T =25 (60mA/ er se)	--	.184	--	W	*1) *2 *3
LE L fet me		Ta 60℃ IF= 0m	--	20 00	--	Hr	*4)

Note1 LED Circu t Dia ram



【Not 2】 A：Anode( )， ：Catho e(—)

【Note3】 ug estio : s ng he onstan current c ntrol o avoid th leakag l ght nd brig tne s quali y issue

【Note4】 Definition of Led life time：Lu inance < In tial umi ance 70%

e

COLO	INPUT DATA	A								D															
		R						R1	R0	G7	G6	G5	G4	G3	G2	G1	0	B7	6	B5	B4	B3	B2	B1	B
		MSB							LSB	MSB							L	MS							LSB
	LACK	0	0		0	0	0			0	0			0	0		0	0		0		0	0		0
	ED 25)		1	1	1	1		1	1	0	0		0	0	0	0	0		0		0	0		0	0
	REEN(55)	0	0	0	0	0	0					1		1	1				0	0	0	0			
B S C	LUE 255)				0					0					0					1					1
C LO	YAN	0	0		0	0	0			1	1	1			1	1	1			1	1	1			1
	M GE TA	1	1	1	1				1					0					1					1	
	E L W		1	1	1	1	1	1	1		1	1	1	1		1	1	0	0		0	0	0	0	
	WHI E	1	1		1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1		1
	RED(0			0					0					0					0				0	
	RED(1			0					1					0					0				0	
	RED( )	0	0	0	0	0				0					0					0					0
R D																									
	R D 2 4)	1	1	1		1	1	1	0	0	0	0	0		0	0	0	0		0	0	0	0		0
	RE (5)	1		1	1	1				0					0					0					0
	R E ( )																								
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GRE N(2)	0	0	0			0	0	0			0	0	0			0	0	0			0	0	0	
GR E																									
	G EE (5)	0		0	0	0	0			1	1				1	1				0	0				0
	R EN 255)	0	0	0			0	0	0			1	1	1			1	0	0			0	0	0	
	LU																						0	0	0
	BLUE( )	0	0		0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0		1
	BLU (2)	0	0	0	0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0		0
B UE																									
	B U (2 4			0		0	0	0		0	0	0			0	0	0			1	1	1			0
	B U (55	0	0	0	0	0	0	0		0	0	0	0		0	0	0	1		1	1	1	1		1

4. INTERFACE CONNECTION

4.1 CN1 (Input Signal)

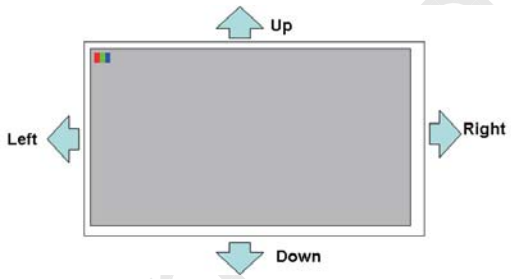
Connector : FH52-60S-0.5SH (HRS)

Pin NO.	Symbol	Description	Note
1	AGND	Analog ground	
2	AVDD	Analog power	
3	DVDD	Digital power	
4	GND	Digital ground	
5	NC	Not connect	
6	DVDD	Digital power	
7	GND	Digital ground	
8	V14	Gamma correction voltage reference	
9	V13	Gamma correction voltage reference	
10	V12	Gamma correction voltage reference	
11	V11	Gamma correction voltage reference	
12	V10	Gamma correction voltage reference	
13	V9	Gamma correction voltage reference	
14	V8	Gamma correction voltage reference	
15	GND	Digital ground	
16	DVDD_LVDS	LVDS power	
17	GND	Digital ground	
18	PIND3	Positive LVDS differential data input	
19	NIND3	Negative LVDS differential data input	
20	GND	Digital ground	
21	PINC	Positive LVDS differential clock input	
22	NINC	Negative LVDS differential clock input	
23	GND	Digital ground	
24	PIND2	Positive LVDS differential data input	
25	NIND2	Negative LVDS differential data input	
26	GND	Digital ground	
27	PIND1	Positive LVDS differential data input	
28	NIND1	Negative LVDS differential data input	
29	GND	Digital ground	
30	PIND0	Positive LVDS differential data input	
31	NIND0	Negative LVDS differential data input	
32	GND	Digital ground	
33	GND_LVDS	LVDS ground	
34	GRB	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10KΩ，C=0.1μF)	
35	STBYB	Standby mode, normally pull high STBYB=” 1” , normal operation STBYB=” 0” ,timing control, source driver will turn off, all output are high-Z	
36	SHLR	Left or right display control	Note 1
37	DVDD	Digital power	
38	UPDN	Up / down display control	Note 1
39	AGND	Analog ground	
40	AVDD	Analog power	
41	NC	Not connect	
42	DITH	Dithering function enable control. Normally pull low DITHER = “1” , Enable internal dithering function DITHER = “0” , Disable internal dithering function	Note 2
43	GND	Digital ground	
44	DVDD	Digital Power	
45	GND	Digital ground	
46	V7	Gamma correction voltage reference	
47	V6	Gamma correction voltage reference	
48	V5	Gamma correction voltage reference	

49	V4	Gamma correction voltage reference	
50	V3	Gamma correction voltage reference	
51	V2	Gamma correction voltage reference	
52	V1	Gamma correction voltage reference	
53	GND	Digital ground	
54	DVDD	Digital power	
55	SELB	6bit/8bit mode select, SELB = “0”, LVDS input data is 8bits SELB = “1”, LVDS input data is 6bits	Note 2
56	VGH	Positive power for TFT	
57	DVDD	Digital power for Gate IC	
58	VGL	Negative power for TFT	
59	GND	Digital ground for Gate IC	
60	NC	Not connect	

Note 1：UPDN and SHLR control function

SHLR	UPDN	Data shifting
DVDD	GND	Left→Right，Up→Down(default)
GND	GND	Right→Left，Up→Down
DVDD	DVDD	Left→Right，Down→Up
GND	DVDD	Right→Left，Down→Up



Note 2: if LVDS input data is 6bits, SELB must be set to High
if LVDS input data is 8bits, SELB must be set to Low

DITH and SELB control function

DITH	SELB	FUNCTION
0	1	Colors (262K)
0	0	Colors (262K)
1	1	Colors (262K)
1	0	16.7M (6bit+2bit HiFRC)

4.2 CN2 (backlight)

PIN NO	SYMBOL	FUNCTION
1	**A**	**Anode**
2	**K**	**Cathode**

Note：

Input connector : BHSR-02VS-1(JST)

Outlet connector: SM02B-BHSS-1(JST)

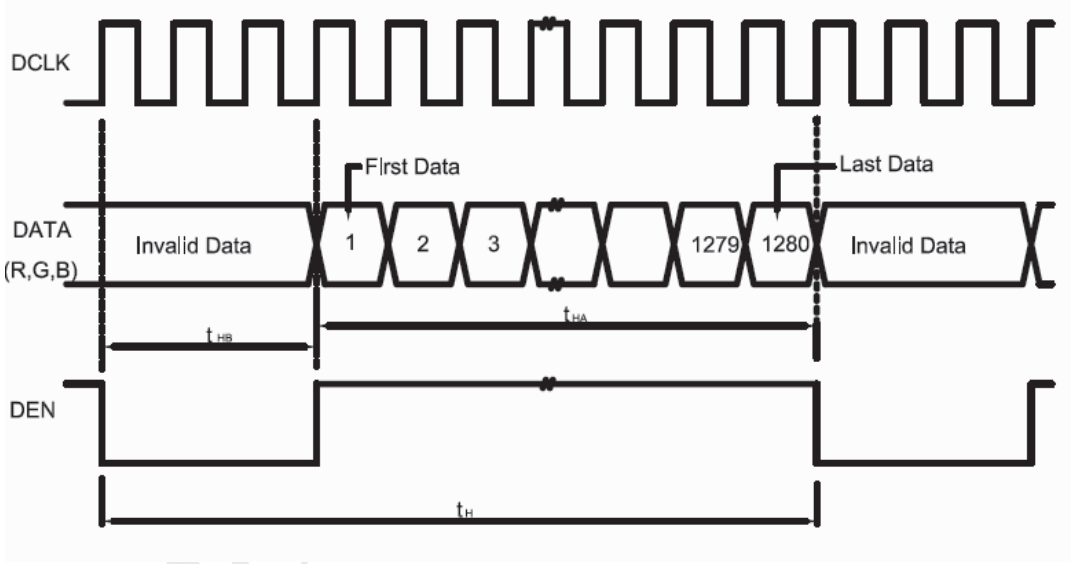
5. INPUT SIGNAL(DE ONLY MODE)

5.1 Timing Specification

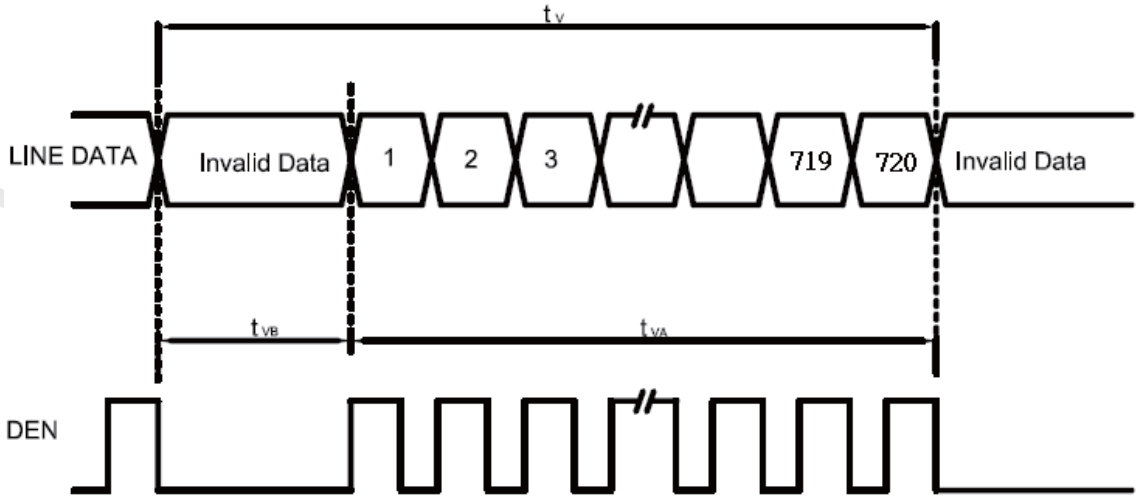
Item				Symbol	Min.	Typ.	Max.	Unit
LVDS input signal sequence	CLK Frequency			1/tclk	63.5	67.3	71.3	MHz
LCD input signal sequence （Input LVDS Transmitter）	DENA	Horizontal	Horizontal total Time	t_H	1450	1480	1500	tCLK
			Horizontal effective Time	t_{HA}	1280			tCLK
			Horizontal Blank Time	t_{HB}	170	200	220	tCLK
		Vertical	Vertical total Time	t_V	730	758	792	t_H
			Vertical effective Time	t_{VA}	720			t_H
			Vertical Blank Time	t_{VB}	10	38	72	t_H

5.2 Timing sequence(Timing chart)

5.2.1 Horizontal Timing Sequence

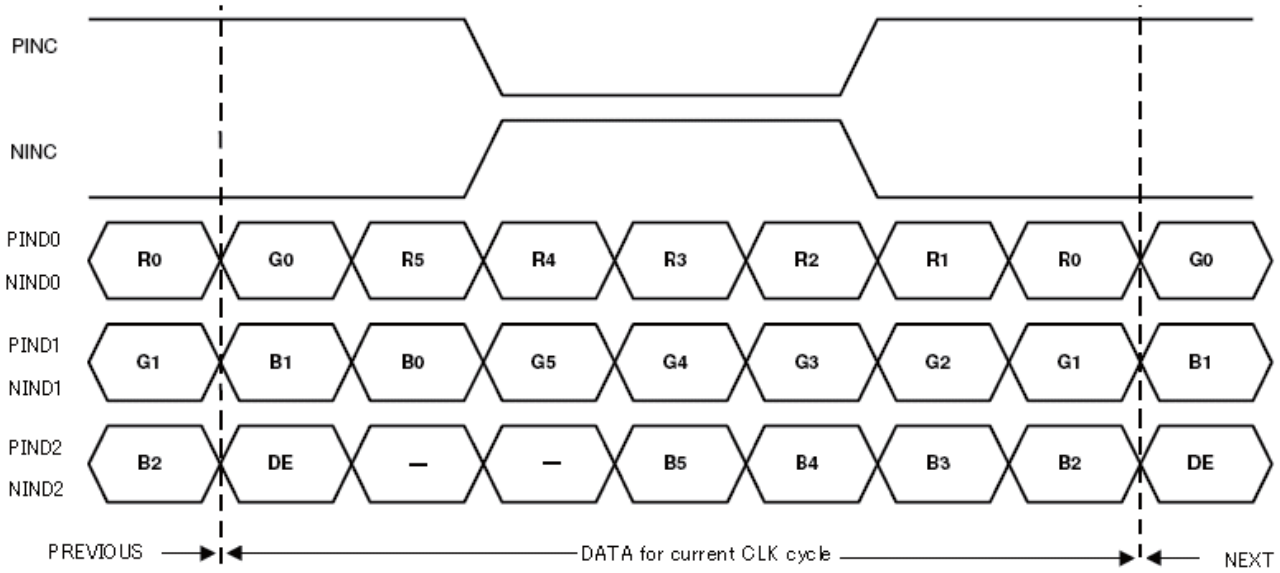


5.2.2 Vertical Timing Sequence

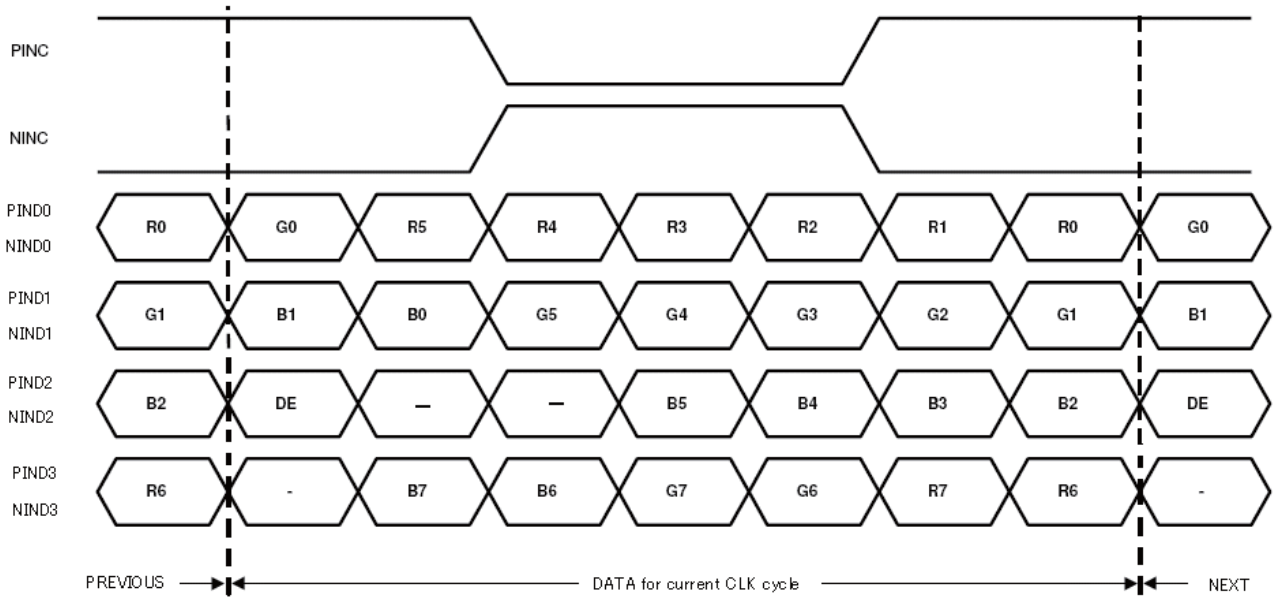


5.2.3 LVDS Input Data mapping

6 Bit LVDS input



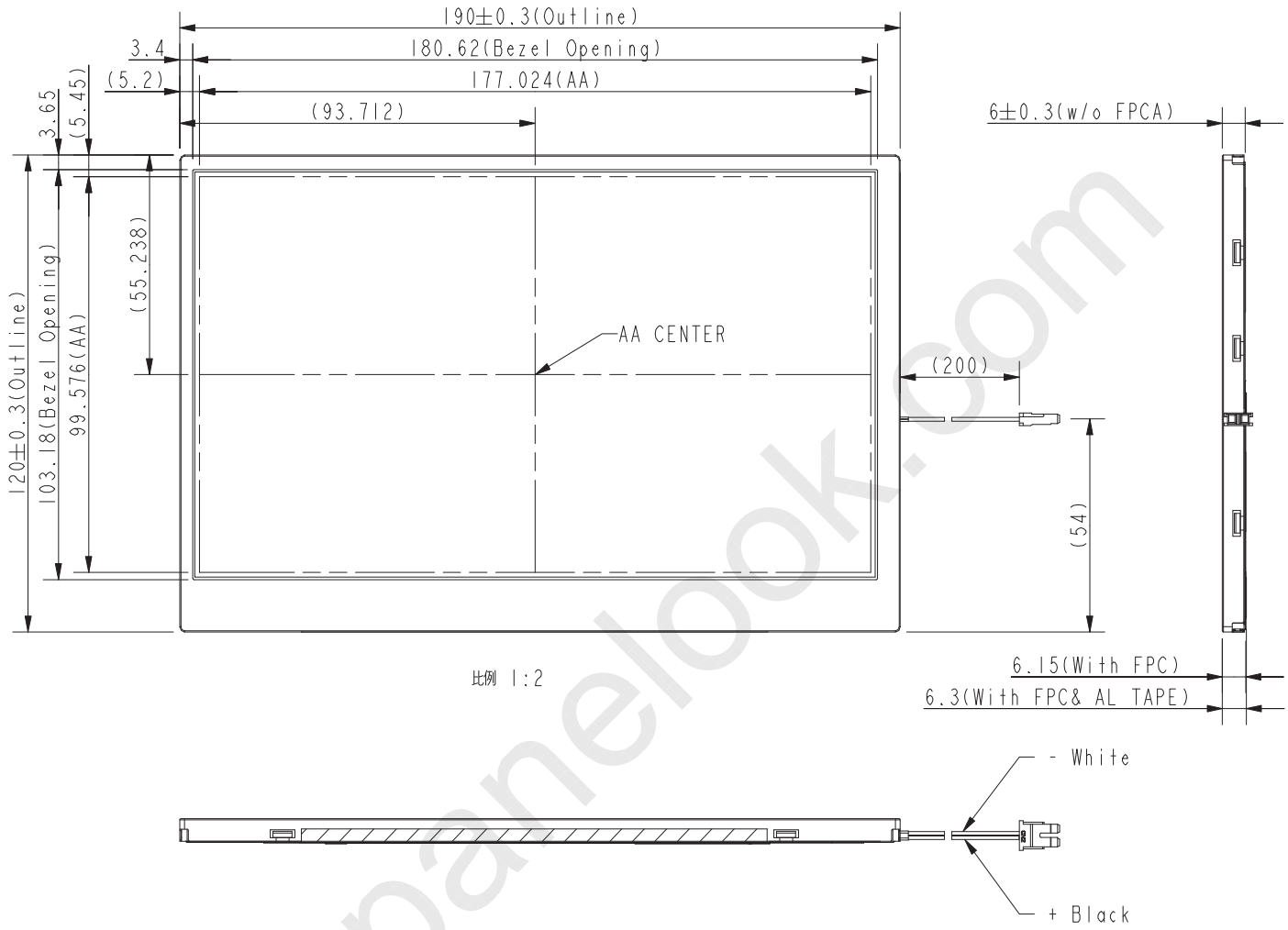
8 Bit LVDS input



6. MECHANICAL DIMENSION

6.1 Front Side

[Unit：mm]



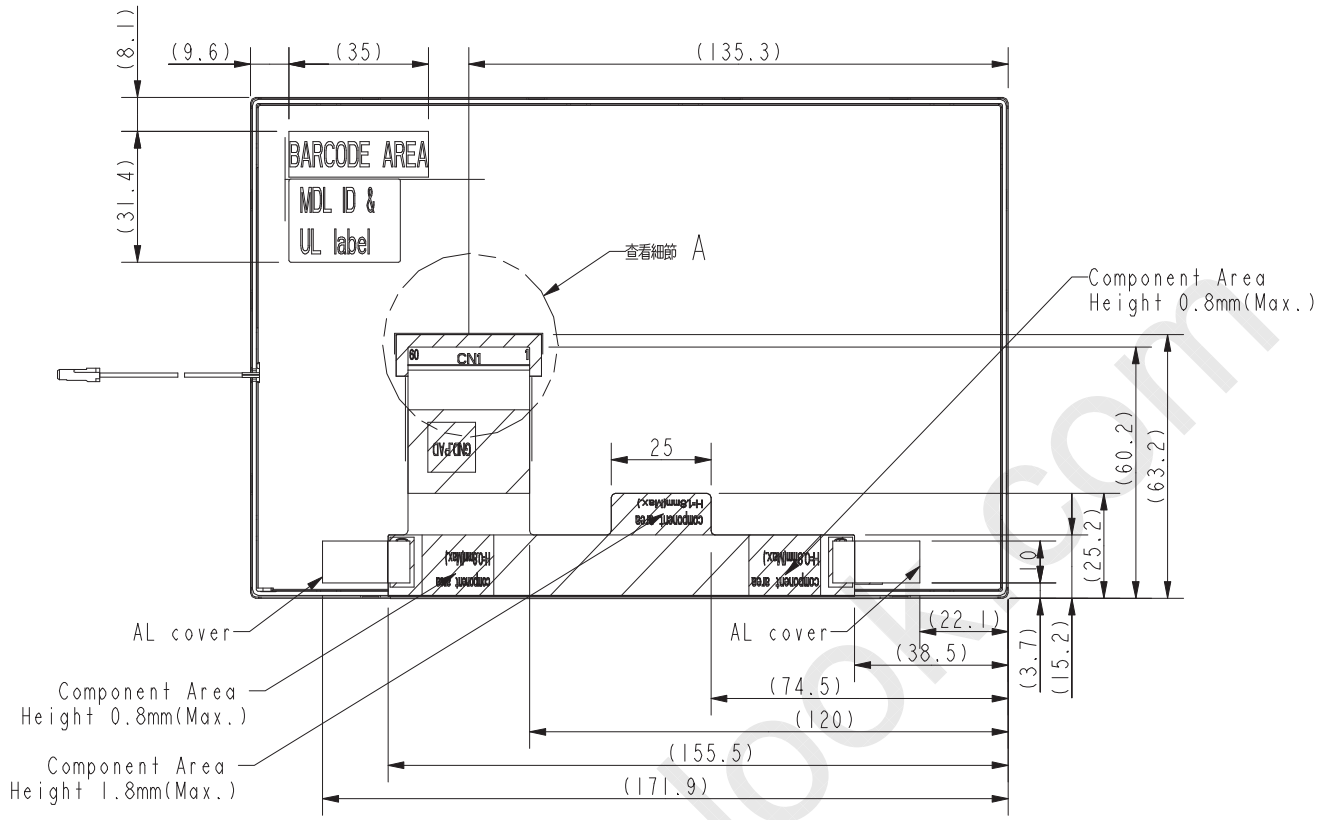
Note：

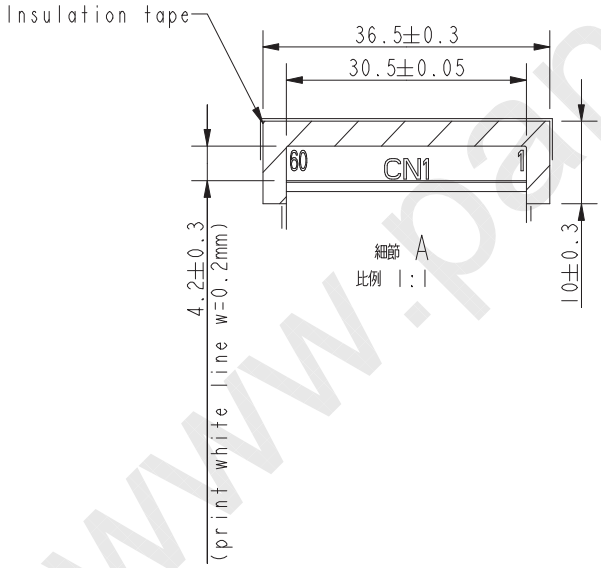
1.General tolerance ±0.3mm

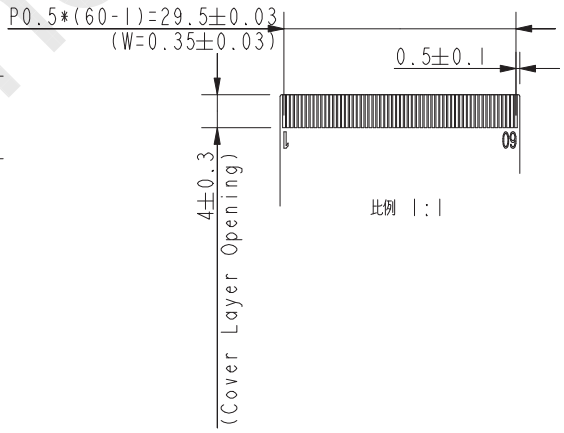
2.CN1 suggested connector(60pin)： FH52-60S-0.5SH (HRS) or equivalent.

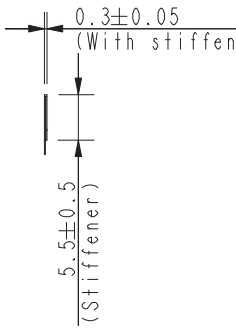
6.2 Rear Side

[Unit：mm]







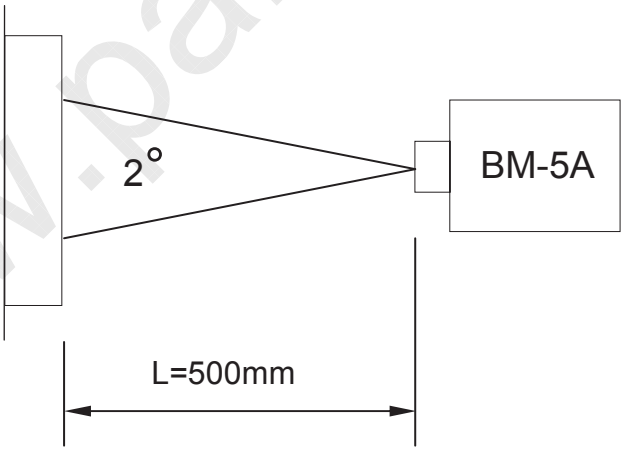


7. OPTICAL CHARACTERISTICS

Ta = 25°C, VCC=3.3V

ITEM		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Constrast Ratio		CR	Point-5	600	900		--	1, 2, 3
Luminance(CEN)		**Lw**	**Point-5**	**400**	**500**		**cd/m^2**	**1, 3**
Luminance Uniformity		**ΔL**		**70**	**80**		**%**	**1, 3**
Response Time (White - Black)		Tr +Tf	Point-5	-	25	40	ms	1, 3, 5
NTSC		-	Point-5	60	70		%	1, 3
Viewing Angle	Horizontal	Left (ϕ)	CR≧10 Point-5	75	85			1, 3
		Right (ϕ)		75	85			1, 3
	Vertical	Up (θ)		75	85			1, 2, 4
		Down (θ)		75	85			1, 2, 4
Color Coordinate	White	Wx Wy	Point-5	0.267 0.284	0.307 0.324	0.347 0.364		1, 3
	Red	Rx Ry		(0.600) (0.307)	(0.640) (0.347)	(0.680) (0.387)		
	Green	Gx Gy		(0.280) (0.595)	(0.320) (0.635)	(0.360) (0.675)		
	Blue	Bx By		(0.111) (0.039)	(0.151) (0.079)	(0.191) (0.119)		

【Note 1】Measure condition：25℃±2℃，60±10%RH，≦1 Lux in the dark room.BM-5A (TOPCON)，viewing angle2°，**IL=180 mA**（**Backlight current**），measurement after lighting on 10 mins.



【Note 2】Definition of contrast ratio：
Contrast Ratio (CR)= (White) Luminance of ON ÷ (Black) Luminance of OFF

【Note 3】Definition of luminance：Measure white luminance on the point 5 as figure.7-1
Definition of Luminance Uniformity: Measure white luminance on the point1~9 as figure.7-1
△L = [L(MIN)/L(MAX)]×100

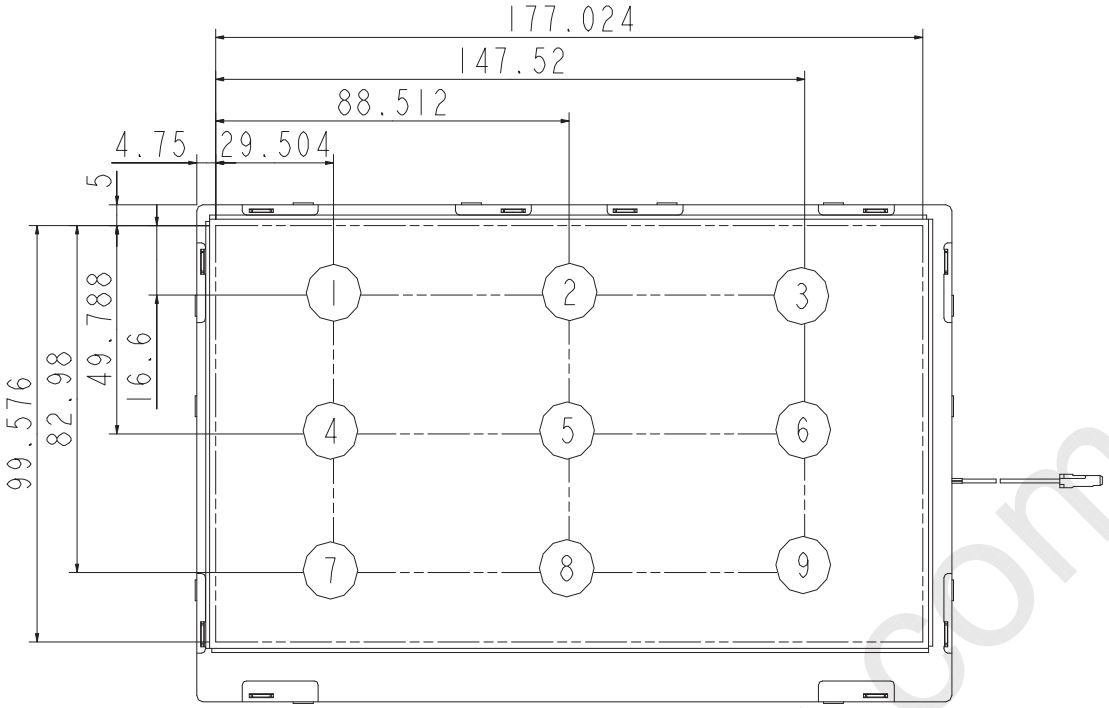


Fig.7-1 Measuring point

Note 4: Definition of Viewing Angle(θ,ψ),refer to Fig.7-2 as below：

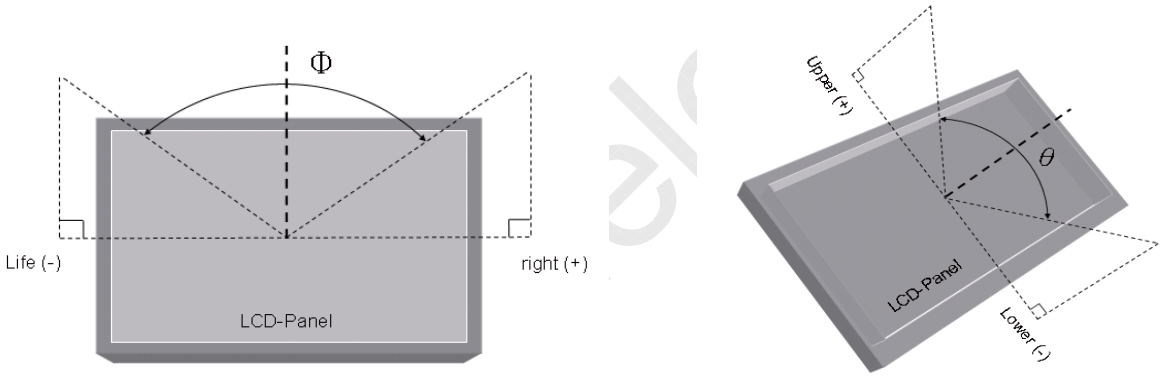


Fig.7-2 Definition of Viewing Angle

Note5: Definition of Response Time.(White-Black)

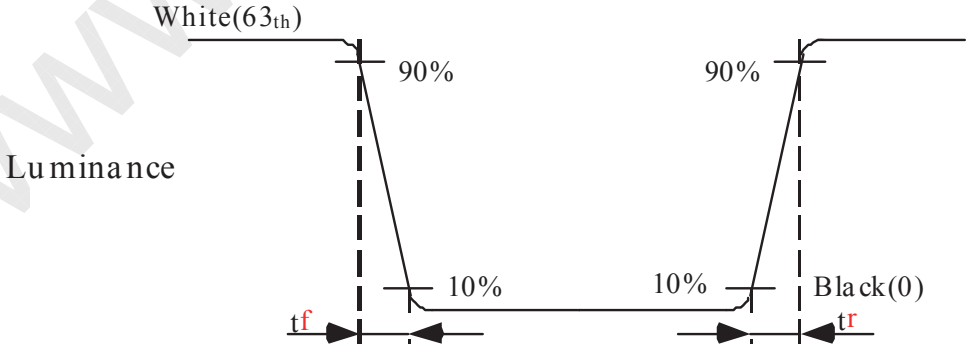


Fig.7-3 Definition of Response Time(White-Black)

8. RELIABILITY TEST

8.1. Temperature and humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	**70℃ ;240hrs**	
High Temperature Storage	**80°C, 240hrs**	
High Temperature High Humidity Operation	**60℃, 90%RH, 240Hrs (No condensation)**	
Low Temperature Operation	**-20°C, 240hrs**	
Low Temperature Storage	**-30°C, 240hrs**	
Thermal Shock	**-20°C(0.5hr) <-> 70°C(0.5hr), 200 cycles**	
Image Sticking	25℃ ; 2hrs	Note 1

【Note 1】：

Condition of Image Sticking test：25 ℃± 2 ℃

Operation with test pattern sustained for 2 hrs, then change to gray pattern immediately.

After 5min, the mura must be disappeared completely .

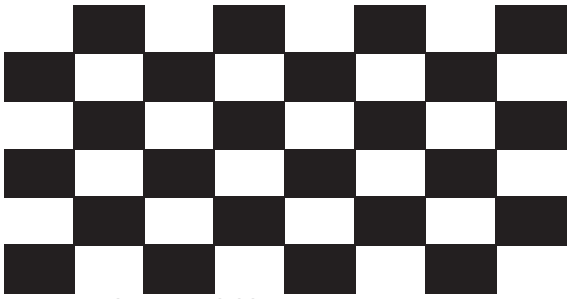
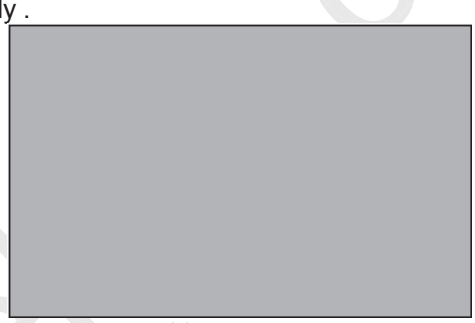


Image sticking pattern



mid-gray pattern

8.2. Shock and Vibration

TEST ITEMS	CONDITIONS
Shock (Non-operation)	● **100G, 6ms,** ● **+X,+Y,+Z，each axis 3 times**
Vibration (Non-operation)	● **Frequency：8~33.3Hz** ● **Stroke：1.3 mm** ● **Sweep：2.9G,33.3~400Hz** ● **Vibration：sin wave, per axis** ● **(both X,Z axis: 2hrs ,Y axis: 4hrs)** ● **Cycle time: 15 min.**

8.3 Electrostatic Discharge

TEST ITEM	CONDITIONS
ESD	[MM] 200pF, 0Ω, ±200V, once for each terminal [HM] 150pF, 330Ω, ±8 & 15kV, 25 times/point, 4points/panel(Air mode) [HM] 150pF, 330Ω, ±8 & 15kV,25 times/point(Contact mode)

8.4 Judgment Standard

The Judgment of the above test should be made as follow:
Pass:Normal display image with no line defect.Partial transformation of the module parts should be ignored.
Fail: No display image, Function NG, or line defects.

9. WARRANTY

9.1 The period is within 12 months since the date of shipping out under normal using and storage conditions.

9.2 The warranty will be avoided in case of defect induced by customer.