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DLC Display Co., Limited

德爾西顯示器有限公司

MODEL No: DLC0350QZG-4

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Record of Revision

Date	Revision No.	Summary
2013-07-23	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0350QZG-4 active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 3.5'' display area contains 320(RGB) x240 pixels.

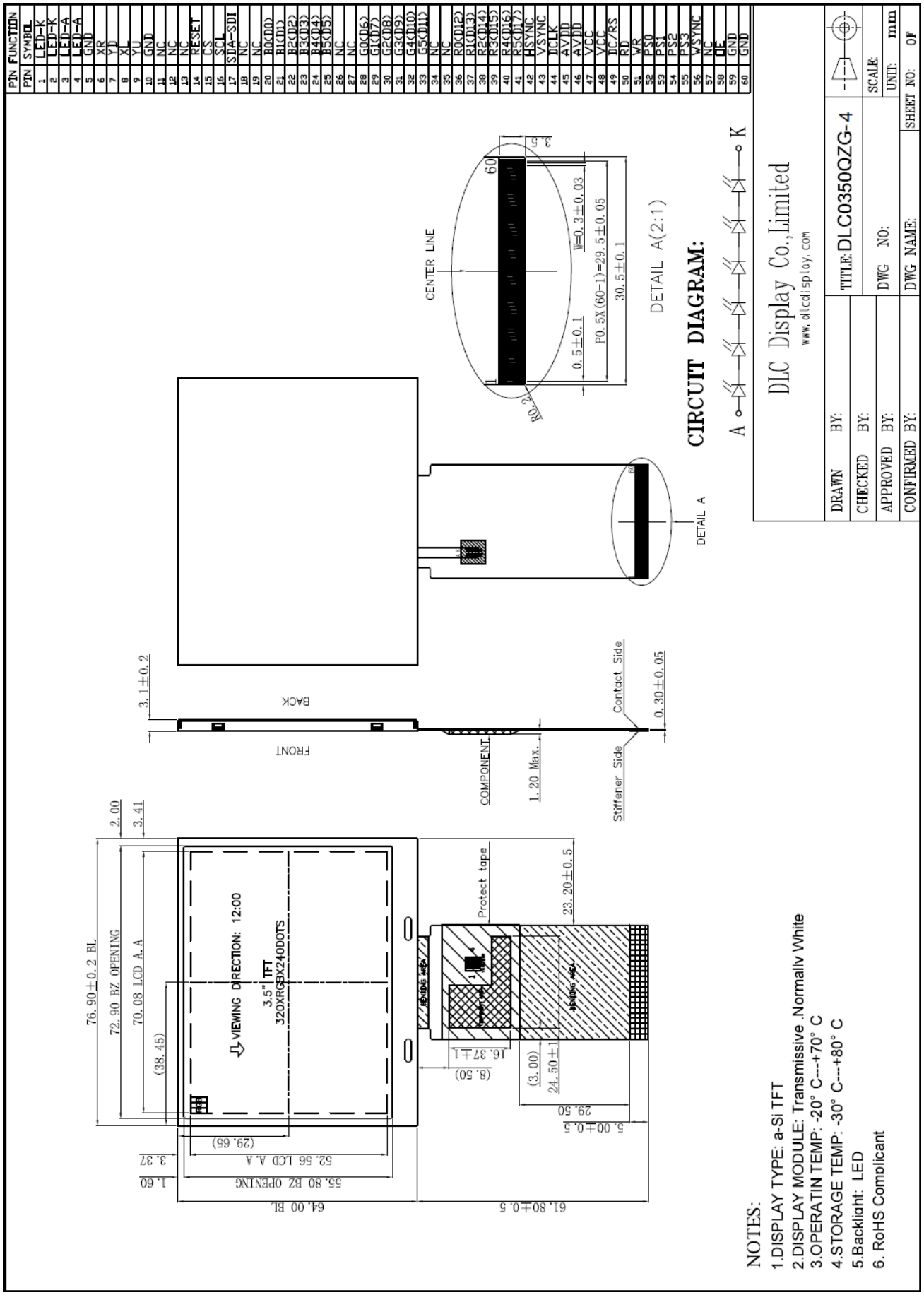
2. Application

Digital equipments which need color display, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	3.5	inch
Resolution	320(RGB) x 240	/
Interface	8/9/16/18-bit Parallel interface & Serial peripheral interface	/
Technology type	TFT	/
Pixel pitch	0.219x0.219	mm
Pixel Configuration	R.G.B. Vertical Stripe	
Outline Dimension (W x H x D)	76.90x64.0x3.1	mm
Active Area	70.08 x 52.56	mm
Display Mode	Transmissive Normally White	/
Backlight Type	LED	/
Driver IC	SSD2119	

4. Outline Drawing



5. Interface signals

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1-2</td><td>LED_K</td><td rowspan="2">Power supply for LED backlight</td></tr>
<tr><td>3-4</td><td>LED_A</td></tr>
<tr><td>5</td><td>GND</td><td>Power supply (system ground)</td></tr>
<tr><td>6</td><td>XR</td><td rowspan="4">Terminal of touch panel.</td></tr>
<tr><td>7</td><td>YD</td></tr>
<tr><td>8</td><td>XL</td></tr>
<tr><td>9</td><td>YU</td></tr>
<tr><td>10</td><td>GND</td><td>Power supply (system ground)</td></tr>
<tr><td>11-13</td><td>NC</td><td>No connection</td></tr>
<tr><td>14</td><td>RESET</td><td>System reset pin</td></tr>
<tr><td>15</td><td>CS</td><td>Chip select pin</td></tr>
<tr><td>16</td><td>SPCLK</td><td>Clock pin of serial interface</td></tr>
<tr><td>17</td><td>SDA-SDI</td><td>Data pin of serial interface</td></tr>
<tr><td>18-19</td><td>NC</td><td>No connection</td></tr>
<tr><td>20-25</td><td>B[0-5]</td><td>Blue data 6-bit/18bit bi-directional (D0-D5)</td></tr>
<tr><td>26-27</td><td>NC</td><td>No connection</td></tr>
<tr><td>28-33</td><td>G[0-5]</td><td>Green data 6-bit/18bit bi-directional (D6-D11)</td></tr>
<tr><td>34-35</td><td>NC</td><td>No connection</td></tr>
<tr><td>36-41</td><td>R[0-5]</td><td>Red data 6-bit/18bit bi-directional (D12-D17)</td></tr>
<tr><td>42</td><td>HSYNC</td><td>Line synchronization signal input</td></tr>
<tr><td>43</td><td>VSYNC</td><td>Frame /Ram synchronization signal input</td></tr>
<tr><td>44</td><td>DCLK</td><td>Dot clock signal</td></tr>
<tr><td>45-46</td><td>AVDD</td><td>Supply voltage for lcd driving</td></tr>
<tr><td>47-48</td><td>VCC</td><td>Supply voltage for logic</td></tr>
<tr><td>49</td><td>DC</td><td>Parallel Interface</td></tr>
<tr><td>50</td><td>RD</td><td>I80 system: Serves as a read signal and reads data at the low level.</td></tr>
<tr><td>51</td><td>WR</td><td>I80 system: Serves as a write signal and writes data at the rising edge.</td></tr>
<tr><td>52-55</td><td>PS[0:3]</td><td>Interface selection pin
<table>
<tr><th>PS3</th><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface mode</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>16-bit 8080 parallel interface, D[17:10]&D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit 8080 parallel interface, D[8:1]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>9-bit RGB(262 colour) + 3-wire SPI, D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB(262K colour) + 3-wire SPI, D[17:10]&D[8:1]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB(262K colour) + 3-wire SPI, D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6-bit RGB(262K colour) + 3-wire SPI, D[8:3]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit 8080 parallel interface, D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>9-bit 8080 parallel interface, D[8:0]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>3-wire SPI</td></tr>
</table></td></tr>
<tr><td>56</td><td>WSYNC</td><td>Ram Write Synchronization output</td></tr>
<tr><td>57</td><td>NC</td><td>No connection</td></tr>
<tr><td>58</td><td>OE</td><td>Display enable pin from controller</td></tr>
<tr><td>59-60</td><td>GND</td><td>Power supply (system ground)</td></tr>
</table>

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage for Logic	VCC---GND	-0.3	4.6	V	
	AVDD	-0.3	4.6		
Power Supply for LCD	VGH-GND	-0.3	18.5	V	
	GND-VGL	-0.3	15		

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

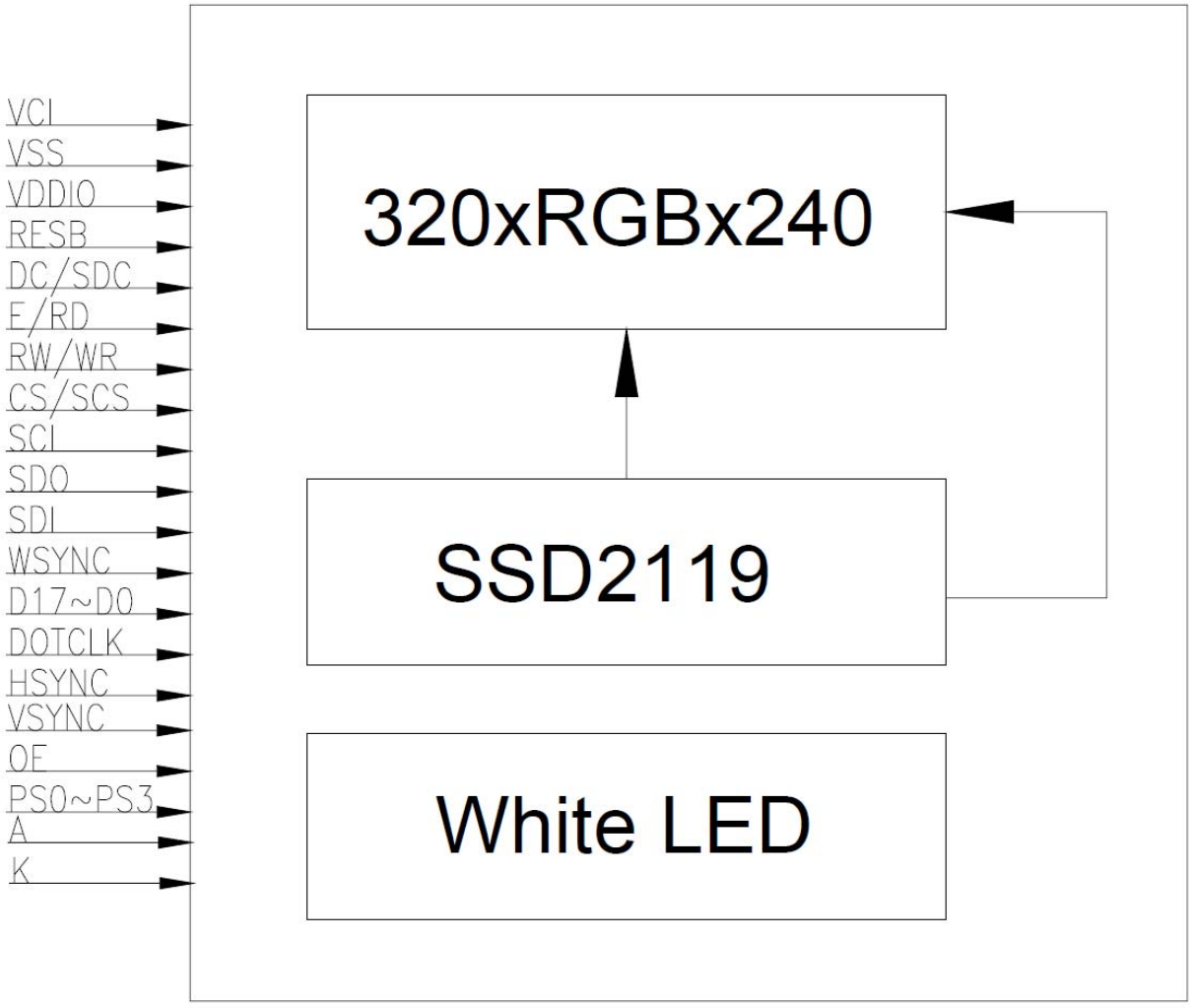
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply	VCC	--	3.3	--	V	
	AVDD	--	3.3	--		
Input Voltage	VIL	0	--	0.3*IOVCC	V	
	VIH	0.7IOVCC	--	IOVCC	V	

7.2 LED Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Voltage	VF	--	19.2	--	V	IF=20mA

7.3 Schematic of LCD module system



8. Command/AC Timing

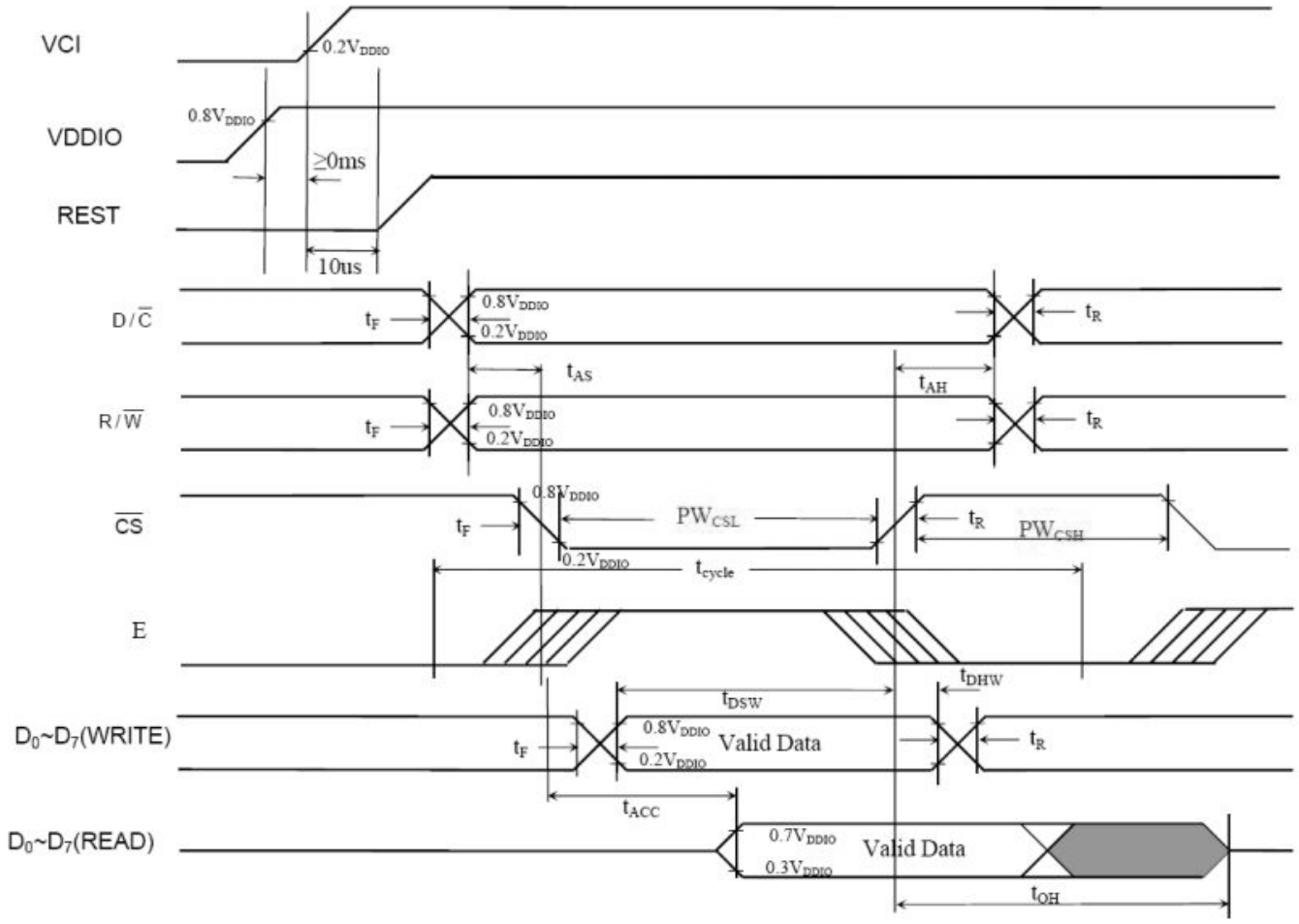
8.1 AC Electrical Characteristics

8.1.1 Parallel 6800-series Interface Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address Setup Time (R/$\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time (R/$\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled



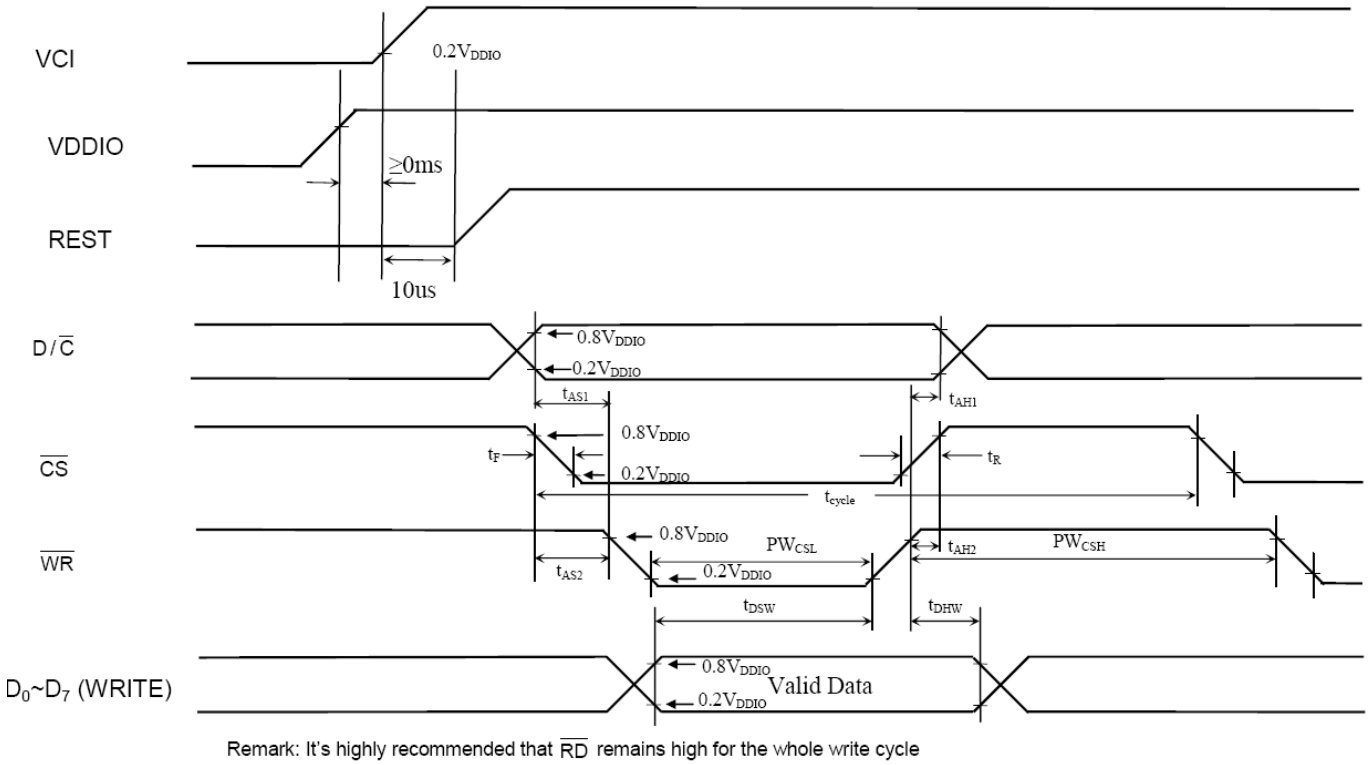
8.1.2 Parallel 8080 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS1}	Address Setup Time between ($R/\overline{W}$) and $D/\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between ($R/\overline{W}$) and $D/\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between ($R/\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between ($R/\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

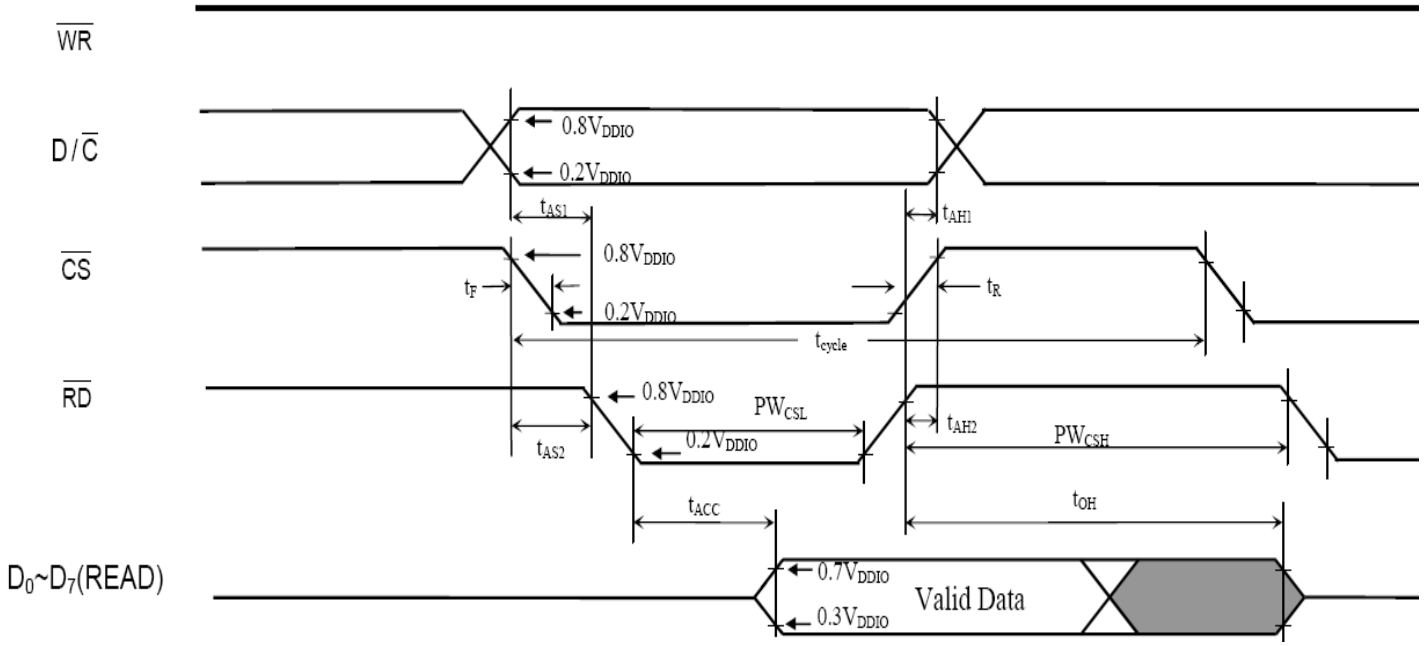
Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle

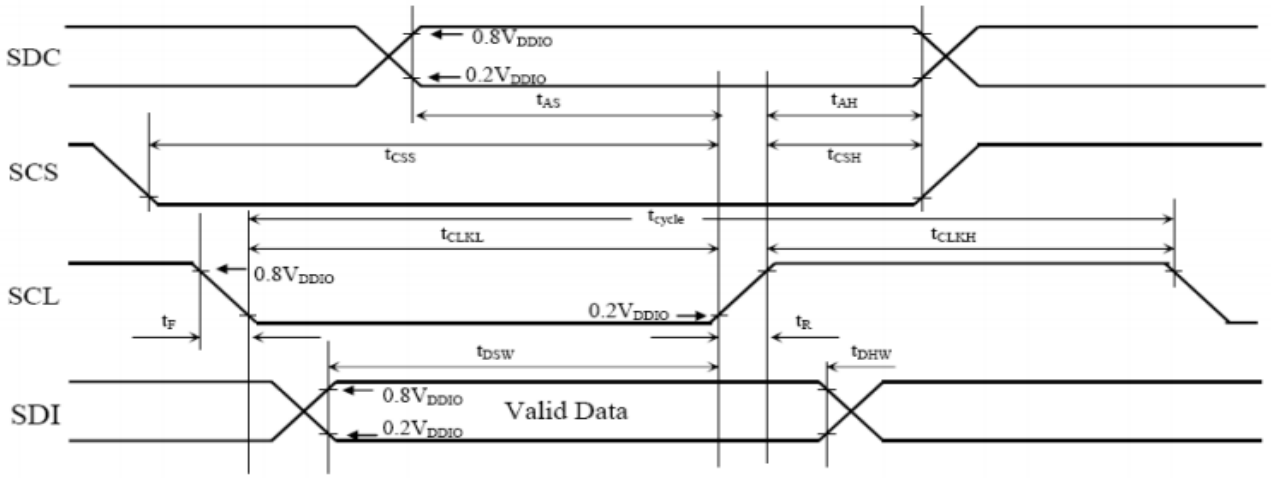

WR
D/C
CS
RD
D0~D7(READ)
0.8VDDIO
0.2VDDIO
tAS1
tAH1
tF
tR
tcycle
tAS2
PWCSL
tAH2
PWCSH
tACC
tOH
0.7VDDIO
0.3VDDIO
Valid Data

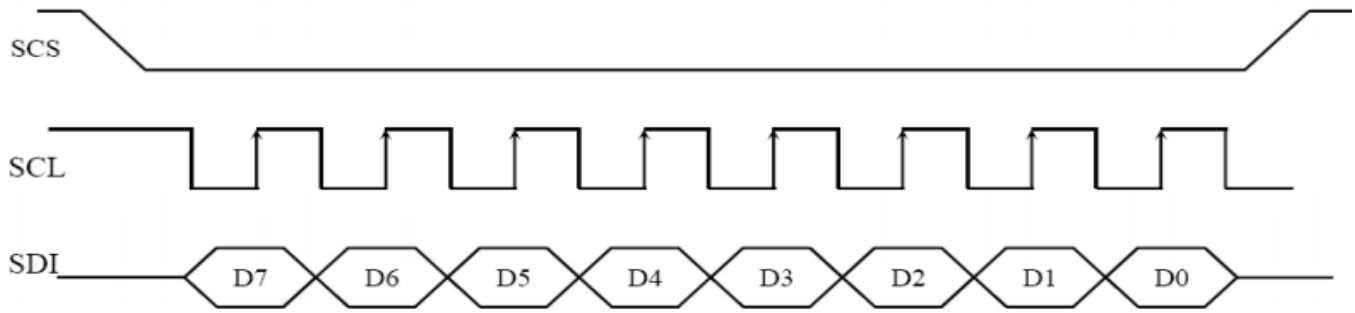
8.1.3 Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

4 wire Serial Timing Characteristics



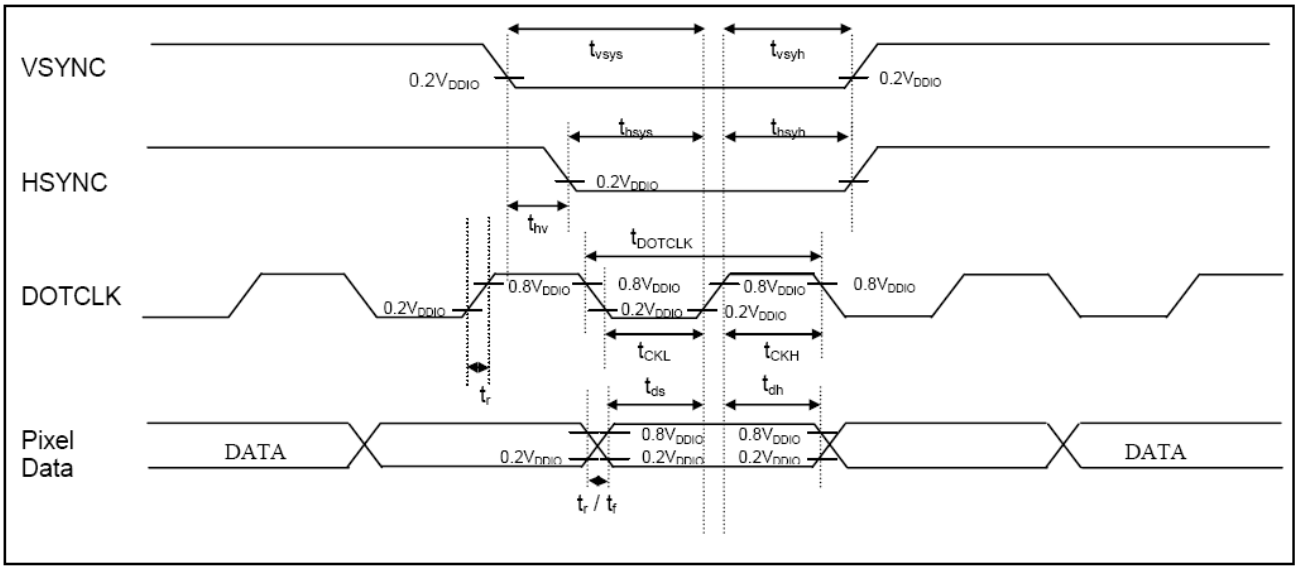


8.1.4 RGB Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns

Note: External clock source must be provided to DOTCLK pin of SSD2119. The driver will not operate in absence of the clocking signal.



9. Optical Specification

Ta=25℃

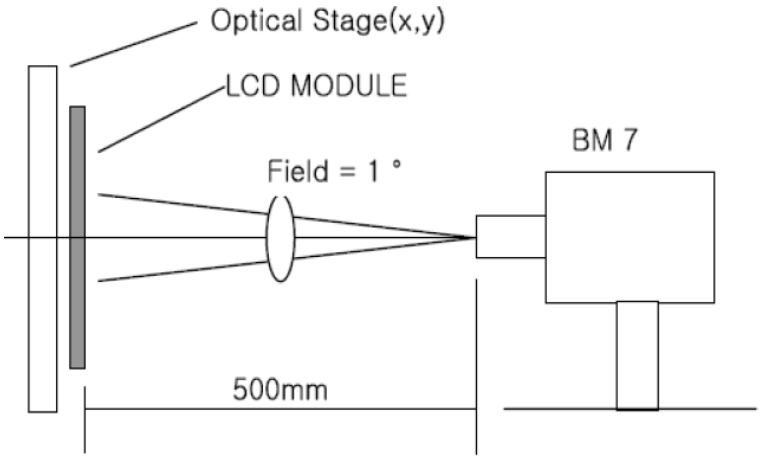
Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	150	250	-		Note1 Note2
Response Time		TR/ TF	25℃	-	50	-	ms	Note1 Note3
View Angles		ΘT	CR≧5	45	60	-	Degree	Note 4
		ΘB		60	70	-		
		ΘL		60	70	-		
		θR		60	70	-		
Chromaticity	White	x	Brightness is on	-	0.31	-		Note5, Note1
		y		-	0.33	-		
Luminance		L		230	270	-	cd/m^2	Note1 Note6
Uniformity		U		70	75	-	%	Note1 Note7

Test condition: IF= 20mA(one channel),the ambient temperature is 25.

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

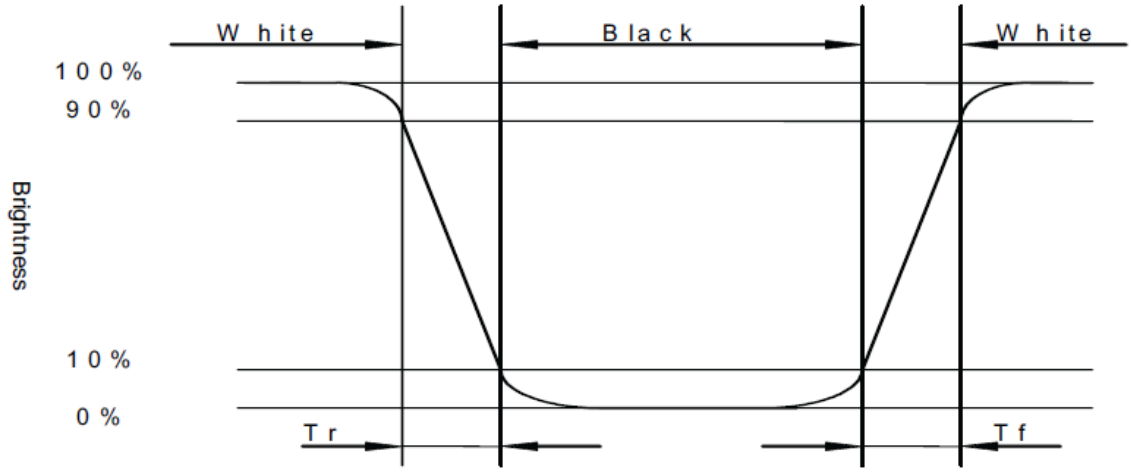


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

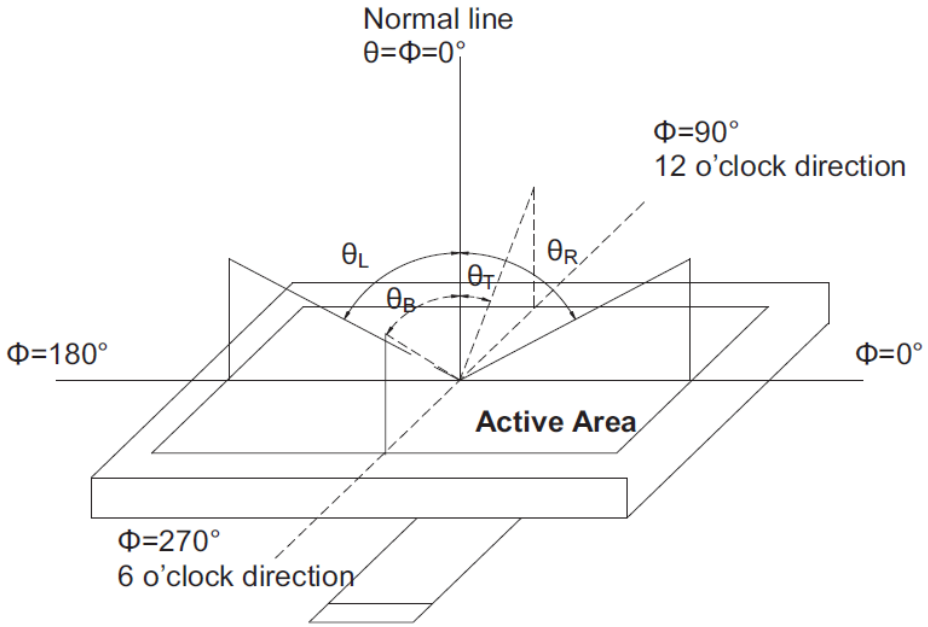
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



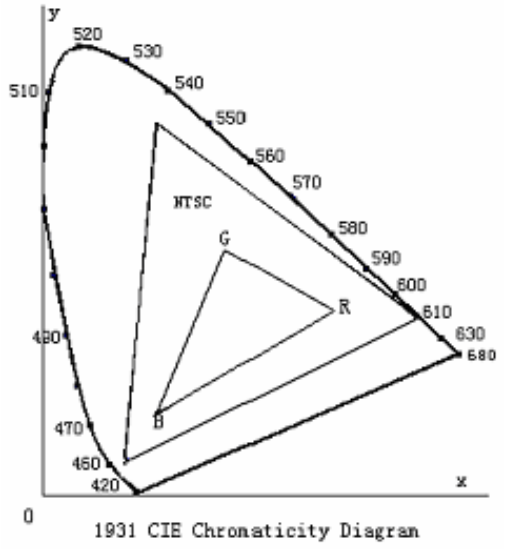
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



1931 CIE Chromaticity Diagram

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

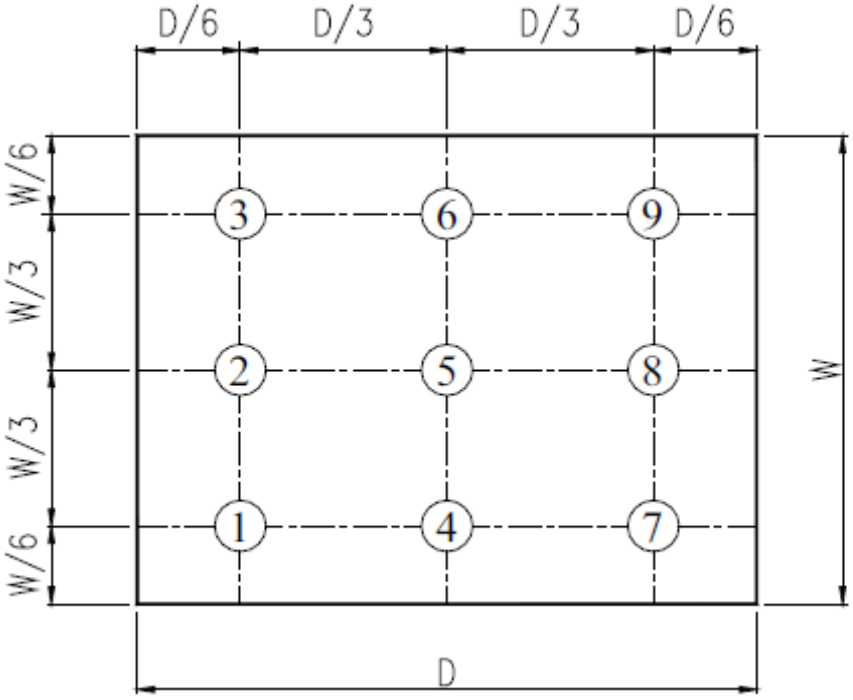


Fig. 2 Definition of uniformity

10.Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+80℃ 120hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+50℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-20℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11.Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.