Using Statistical Process Control with Automatic Test Programs

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Many program managers are struggling with trying to meet their requirements with a declining budget. Statistical Process Control (SPC) is a tool that may help program managers get a greater return on investment. This study used historical test information to determine whether SPC should be used as a normal part of developing and supporting automatic test programs. The findings suggest that significant cost savings, with increased quality, can be gained by using SPC techniques.

Statistical process control is a method that allows users to separate random variations in their data from nonrandom variations, then analyze the nonrandom variations to improve the quality and reduce the cost of products. Conservative calculations in this article suggest that program managers can save millions of dollars over the life of a weapon system by applying statistical process control theory to automatic test programs. In this article, I use historical test data to show how statistical theory can be used to improve test programs. It is intended for readers with some basic knowledge of statistics but does not get into mathematical derivations because commercial applications ranging from spreadsheets to statistical process control products can perform the statistical calculations.

In my experience, SPC has been an overlooked tool in supporting the test programs associated with Automatic Test Equipment (ATE). Because of my success with SPC techniques in the field of ATE and circuit cards, these are used in the examples. However, SPC techniques can be applied to many other areas in which the user can break the repeatable process down so that the statistics can be applied to well-defined, repeatable, and measurable steps.

Advantages of Using SPC Techniques

There are many advantages to using SPC techniques during the development and maintenance of test programs. SPC techniques identify the true performance capability of the test program in relationship to the circuit card's performance and the test station's ability to test the circuit card. The use of SPC techniques will help reduce the overall lifecycle cost associated with the test program, including

- Eliminating or reducing the possibility of performing repair actions on a good circuit card.
- Reducing the chance of changing tolerances that would allow a faulty circuit card to pass.
- Reducing the chance of sending a faulty circuit card to the supply system as a good asset.
- Eliminating or reducing the tweaking of tolerances and test procedures that occur over the life of a test program, usually one at a time. By contrast, all of the potential problems identified through these techniques could be addressed in a single software update.
- Ensuring invaluable information is available if the tested item ever becomes obsolete. If a circuit is redesigned, it would be logical to assume the design engineer would design the new circuit to perform at the center of the testing tolerances. There is a potential that the new circuit will not function properly in the system if the older circuit performed closer to the edge of the tolerance.

The following example shows how you can estimate your potential savings by requiring the use of SPC techniques. Data for your specific project would be needed to determine your potential savings.

- Assume, for instance, that on the average, the use of SPC identifies 10 *changes* that need to be made on the test programs (C = 10).
- Assume that you are managing 100 analog *test* programs (T = 100).
- Assume there is an average $10,000 *price* per software update (P = $10,000).

If the problems are identified and corrected one at a time, your cost is

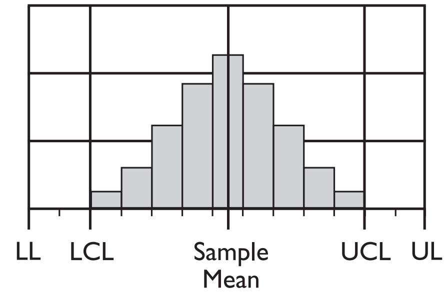
C*T*P or 10 * 100 * $10,000 = $10 million

If, by using SPC techniques, all problems are identified and corrected in a single update, the cost to the program manager is T*P = 100 * $10,000 = $1 million. This saves you $9 million in software updates. These calculations do not include the potential savings from reducing the rework costs.

Where to Start

To begin using statistics to control processes, you should identify what should be measured, the sampling method, and the data that exists. Statistics can be applied to both the product and the process. The product data includes conformance to specifications, whereas the process data includes the cost, schedule, and defect data. To use statistics on the process, the user must be able to break

Figure 1. *The desirable relationship is for control limits to be inside the test limits.*



the process down so that the statistics can be applied to well-defined, repeatable, and measurable steps.

The Sampling Method

It is often cost prohibitive to perform a manual measurement on every product produced. In this case, you need to address a method of using sample sets, such as randomly sampling 10 units every week. In other cases, automated systems may give you a 100 percent sampling capability.

Existing Data

In the case of process data, it is often difficult to determine exactly what should be measured, how to measure it, and how to display the data in a useable manner. When implementing the SPC concept, you may immediately develop new measurement schemes to capture "useable" data. Then, after taking process measurements over time, you may find that the data you are gathering is not giving you the information you want. Applying statistical theory to the existing data will help guide you when making changes to how the events are measured.

SPC Review

The run chart and histogram are two of the easiest methods to display historical data. These two charts provide much information about each of the tests performed on the circuit card. The histogram in Figure 1 shows the desirable relationship between the upper and the lower test limits (UL and LL) in comparison to the upper and the lower process control limits (UCL and LCL). The desirable relationship is for the control limits to be within the limits defined by the test program.

When the control limits fall outside of the test limits, as shown in Figures 2 through 4, many items will be reworked, thrown away, or salvaged for parts, resulting in higher production costs. The process may also incur additional intangible costs. An example of an intangible cost is customer dissatisfaction, which may result from paying excessive costs, lengthy delays, poor quality, or receiving faulty products. When the control limits fall outside of the test tolerances, as shown in Figures 2 through 4, the following questions should be asked.

- Can the manufacturing process or (in the case of ATE) the repair process be changed to reduce the rework costs and improve the quality?
- Are the specification limits correct?

Applying SPC Concepts to Our ATE Test Programs

ATE Test Tolerances

The derivation of the ATE test tolerances for electronic circuits can typically be traced to one of the following three methods.

- The parameter was specified in the original design requirement.
- A calculation was made to determine the theoretical performance of the circuit. This could be the result of a manual calculation or a computer circuit simulation.
- A measurement was made on a good circuit card, often called a "golden board," and then a +/-n% tolerance was added to the measurement.

Figure 2. *An undesirable condition – the lower control limit is less than the lower test limit.*

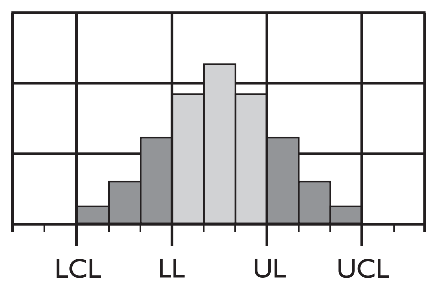


Figure 3. *An undesirable condition – the upper control limit is greater than the upper test limit.*

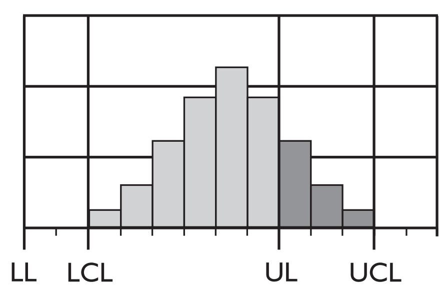
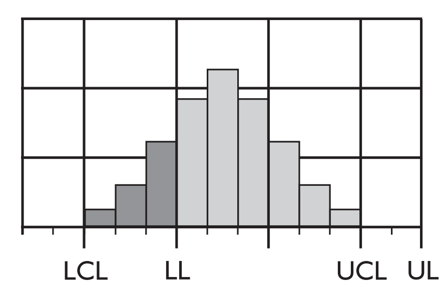


Figure 4. *An undesirable condition – both test limits are inside the control limits.*



From an SPC viewpoint, none of the methods discussed above will identify the capabilities of the circuit and the test station's ability to test the circuit. The verification of the system design is based upon a First Article Test, which usually verifies only that the system meets the design requirements. The number of inputs and outputs tested at the system level may be significantly less than the total number of input and output pins on all of the circuit cards internal to the system.

This problem is further complicated when the government test program is not hosted on the factory test equipment. The attributes of the ATE may be different on the depot test station than they were on the factory test equipment. The test station's attributes, such as input impedance, cross talk, and insertion loss, have a direct impact on the results of the test. Typically, the ATE attributes are not considered when the test specifications are developed for a circuit card.

Data and Assumptions

During this study, I was fortunate to be able to collect approximately two years of test results for a particular type of circuit board. Approximately 195 circuit cards of the same type were tested during this time. Surprisingly, our ATE does not provide us with an easy means to capture the test results and store the information into a format that can be easily used. Commercially available ATE may provide this capability, but I am unaware of any ATE specifically designed for use with a government weapon system that provides this capability.

The historical test results did not include the UUT serial number, which may have resulted in the same item appearing more than once. I assumed that once all of the tests passed, the station operator would not rerun the test program on the same UUT. I also lim-

Terminology

Common terms and acronyms used with statistics and ATE.

ATE: Automatic Test Equipment, which is used in this case to test electronic circuit cards.

UUT: Unit Under Test, e.g., the electronic circuit card being tested.

TPS: Test Program Set, which includes the software necessary to test the circuit card and the interface device between the circuit card and the test station.

LL: Lower limit defined in the test program. The LL may also be called the lower test limit.

UL: Upper limit defined in the test program. The UL may also be called the upper test limit.

TEST Number: This number, such as Test 791007, refers to the programmer-defined file statement number in the source code of the test program.

Mean (m): The average of the samples.

Standard Deviation (s): A way to show how the samples are distributed in relation to the sample mean. For a normal distribution, 68 percent of the samples are within m +/- 1s, 95 percent of the samples are within m +/- 2s, and 99.7 percent of all samples are within m +/- 3s.

LCL: Lower Control Limit, which for this study I set for the process at m - 3s.

UCL: Upper Control Limit, which for this study I set for the process at m + 3s. Statistically, 0.3 percent of the measurements will fall outside of the range I selected to calculate the LCL and UCL. Measurements outside of the control limits do not necessarily indicate that there is a problem; further analysis is required to determine whether there is a problem with the process.

Sample Set: Often, it is economically unfeasible to perform a 100 percent sampling of the products being produced. Statistics allow the user to perform a random sample, such as randomly testing 10 items at the end of every week. Through the use of statistics, the user can predict, with a reasonable certainty, the attributes of the unmeasured items based upon the results of the items that were measured. The X(bar) and R control charts are commonly used when the data is gathered in sample sets.

Histogram: The histogram is a way to graph the frequency (how often) the measurement occurs. The histograms in this article were graphed so that the LL corresponds to the left side of the histogram and the UL corresponds to the right side of the histogram.

Run Chart: A simple way to graph each measurement as it is made. Adding both the control limits and the test limits to the run chart provides an easy way to compare the information.

R Chart: A graph of the range (difference) between the largest and the smallest measurement in each sample set taken over time.

X(bar) Chart: A graph of the average of each sample set taken over time.

ited the data to only the test program executions that resulted in a UUT-passed message. This gave me an indication of the condition of the UUTs when they were returned to supply as serviceable. To perform a study of this nature, I recommend that the following information be collected for each test.

- Date and time.
- UUT part number and serial number.
- Test station serial number (if more than one may be used).
- Test number.

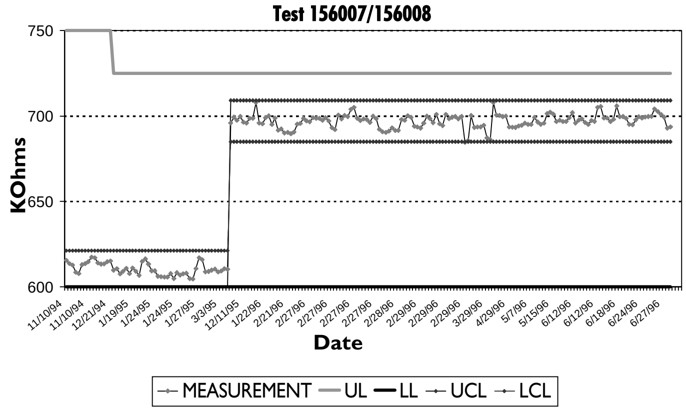


Figure 5. *The run chart can be used over time to show the results of the measurements and the effects of process changes.*

- Measurement and the units (such as ohms and VDC).
- Upper and lower test limits.
- Pass or fail information.

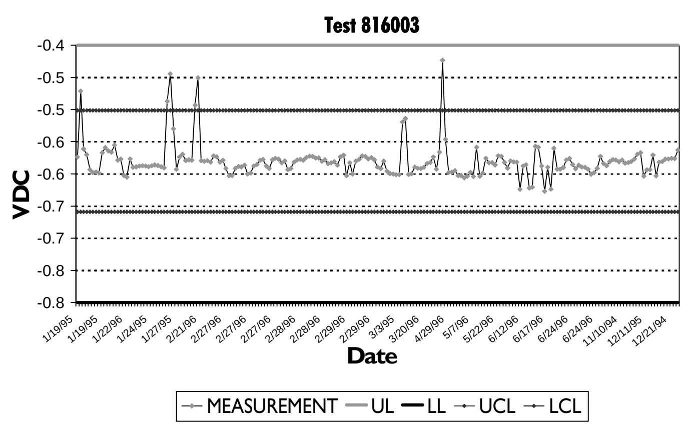
Process Changes

When calculating the upper and the lower control limits, it is important to take into account process changes. The run chart in Figure 5 shows that the UL was lowered in early 1995, and a second software change was made in early 1996. The first change had no effect on the measurements being taken or on the process control limits. The second software change had a significant impact on the measurements, which in turn shifted the process control limits. The measurements shifted from the lower end of the test limits toward the upper end of the test limits.

The first set of process control limits, UCL_1 and LCL_1, were calculated using only the measurements taken before the process change in 1996. The second set of process control limits, UCL_2 and LCL_2, were calculated using only the measurements taken after the process change in 1996. The process capability would appear to be much wider, and therefore worse, if the standard deviation was calculated using all the measurements in a single calculation.

Displaying the run chart as shown in Figure 5 allows for a quick visual comparison of the process capabilities in relation

Figure 6. *The run chart can be used to spot anomalies in the test data.*



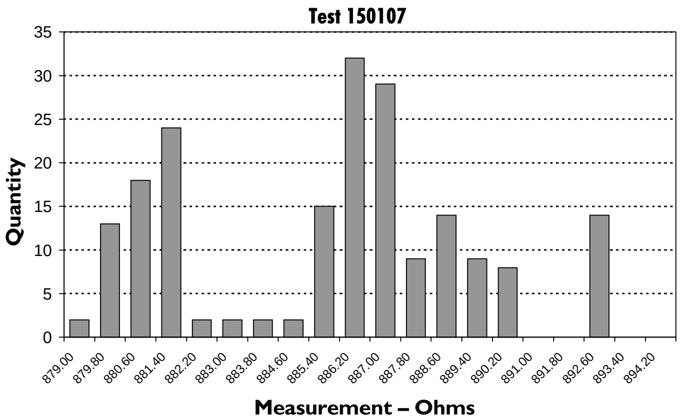
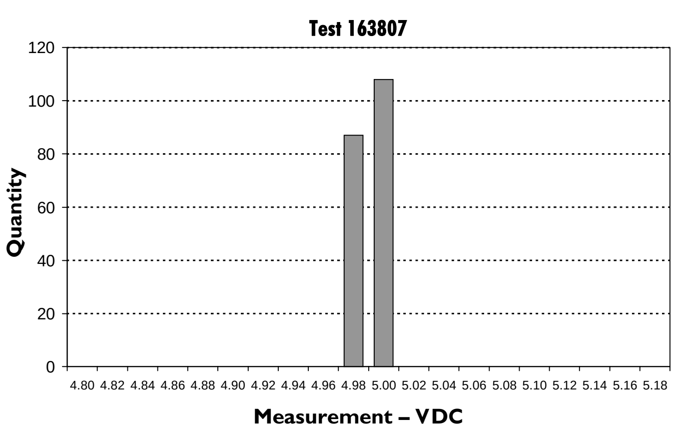


Figure 7. *The run chart for test 150107 shows three peaks in the measurements.*

to the test limits. This chart is a good example of how the use of SPC techniques may have driven a different outcome than the software changes associated with the two software releases. In the first software change, the programmer lowered the upper test limit. I was unable to locate the documentation associated with the change, but I assume the change was probably driven by a UUT that failed in the next higher assembly, yet passed at the upper margin of the test tolerances.

In a similar manner, I believe that the second change was made because good assets were falling slightly below the lower limit. The lower control limit at that time was lower than the lower test limit. In the second change, the programmer chose to add a delay to the program and change the scale on the multimeter. The result of the second change is the sample mean shifted from the lower edge of the tolerances toward the upper edge of the tolerances. The range between the upper control limit and the lower control limit was basically the same. I suspect that if this run chart had been available when the first software change was made in 1995, both the upper and the lower test limits would have been analyzed in more detail, and a different solution would have been implemented.

Figure 8. *This test measures the 5VDC applied to the circuit card. All of the measurements for the bar on the left were taken on station No. 5; all measurements for the bar on the right were taken on station No. 2. In this case, the minor calibration difference between the two stations does not negatively impact the test results.*



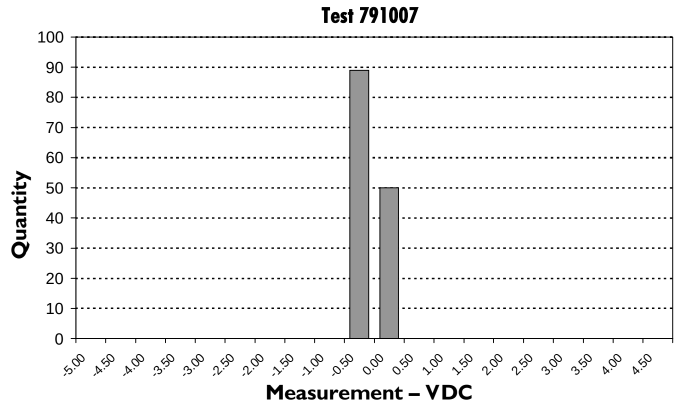


Figure 9. *Is this too good to be true? The process capability ratio (UL - LL) / (UCL - LCL) = 1250. Note: This equation is slightly different from the more familiar C_{PK} equation.*

The second software change in 1996 would not have been required.

Test 816003 (Figure 6) matches the desirable relationship discussed with Figure 1. Statistically, I expected 0.3 percent of the measurements to fall outside of the control limits. If the test limits are correct, I can be confident that the six circuit cards that measured between the upper control limit and the upper test limit will work properly in the system. The SPC user will be able to spot potential problems by watching these anomalies in the data. Problems with substitute parts, drifting calibrations, and aging or degrading components can be detected by looking for nonrandom anomalies and trends in the data.

Multiple Peaks in the Data

The use of multiple vendors or multiple measurement devices may cause peaks and valleys in the histogram, as shown in Figures 7 and 8. These peaks are another indicator that there may be a problem with the process. Identifying the causes of the peaks can be used to improve the procedures for procure parts, improve the procedures to calibrate the test equipment, etc.

Process Capability

The run chart and histogram can also show a cause for concern when the process capability is too good to be true, as is the case with Figure 9 for Test 791007. The tolerances for this test may be too wide; the program allows for a 10.000 VDC range between the lower and the upper test limit (-5.0 VDC to + 5.0 VDC). The data revealed that the range for the 139 circuit cards tested was only 0.0008 VDC between the lowest reading for the bar on the left (89 samples) and the highest reading for the bar on the right (50 samples). Knowing this information, I would suspect that I had a bad circuit card if it measured 4.50 VDC.

Need to Take Your Project's Temperature?

Good software development requires good data on project status—without it, your project could be suffering any number of diseases and you wouldn't know until too late.

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Results of the Study

Sixty-five tests for one UUT test program were analyzed in this study. The first three findings discussed below relate to Figures 2 through 4. Both the repair process and the testing tolerances should be reviewed for Findings 1 through 3 to determine whether the excessive rework could be reduced or eliminated. Reducing the rework effort results in lower costs to the customer. The findings included:

- In nine of the 65 tests, the LCL was less than the LL.
- In seven of the 65 tests, the UCL was greater than the UL.
- In three of the 65 tests, both the upper and the lower control limits were outside of the testing limits.
- Thirty-four of the 65 tests resulted in ratios of the test limits to the control limits (UL-LL) / (UCL-LCL) greater than five. This suggests that further analysis should be performed to determine if the tolerances are too wide and allowing faulty circuits to pass.
- Using the equation (Sample Mean – Center of test limits) / (3 standard deviations) revealed that for 13 of the 65 tests, the sample mean was shifted from the center of the tolerances by more than three standard deviations. This also suggests that further analysis should be performed to determine if the tolerances are correct. Genichi Taguchi and many other quality experts stress that the cost of quality rises if the process is not centered within the tolerances.

Conclusions

SPC techniques should be used as a tool to support test programs on automatic test equipment and similarly structured work, because conservative calculations suggest that millions of dollars could be saved by applying these techniques. Resistance to change or a reluctance to admit that the previous process was not perfect may hinder efforts of this nature. Program managers, shop operators, and engineering staff need to work together to assure that data is collected and used in an optimum manner. They also need to assure that future ATE procurement activities guarantee that the test results can be easily captured, manipulated, and displayed as shown in this article. ◆

About the Author

David B. Putman is lead of the Software Engineering Process Group in the Software Engineering Division at Hill Air Force Base, Utah. He has over 17 years experience in ATE, two years with Hughes Aircraft and over 15 years with the Air Force. He was the senior engineer within the Avionics Software Support Branch for nine years, and he supervised ATE engineering teams for two years. He also supervised the F-16 Operational Flight Program System Design and Integration Test teams for one year. He has a bachelor's degree in electrical engineering from the University of Utah and a master's degree in business administration from Utah State University.

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